

# Compal Confidential

EL434/EL534/EL5C4(C340/S340)

DIS M/B Schematic Document

Intel Comet Lake Processor with DDR4

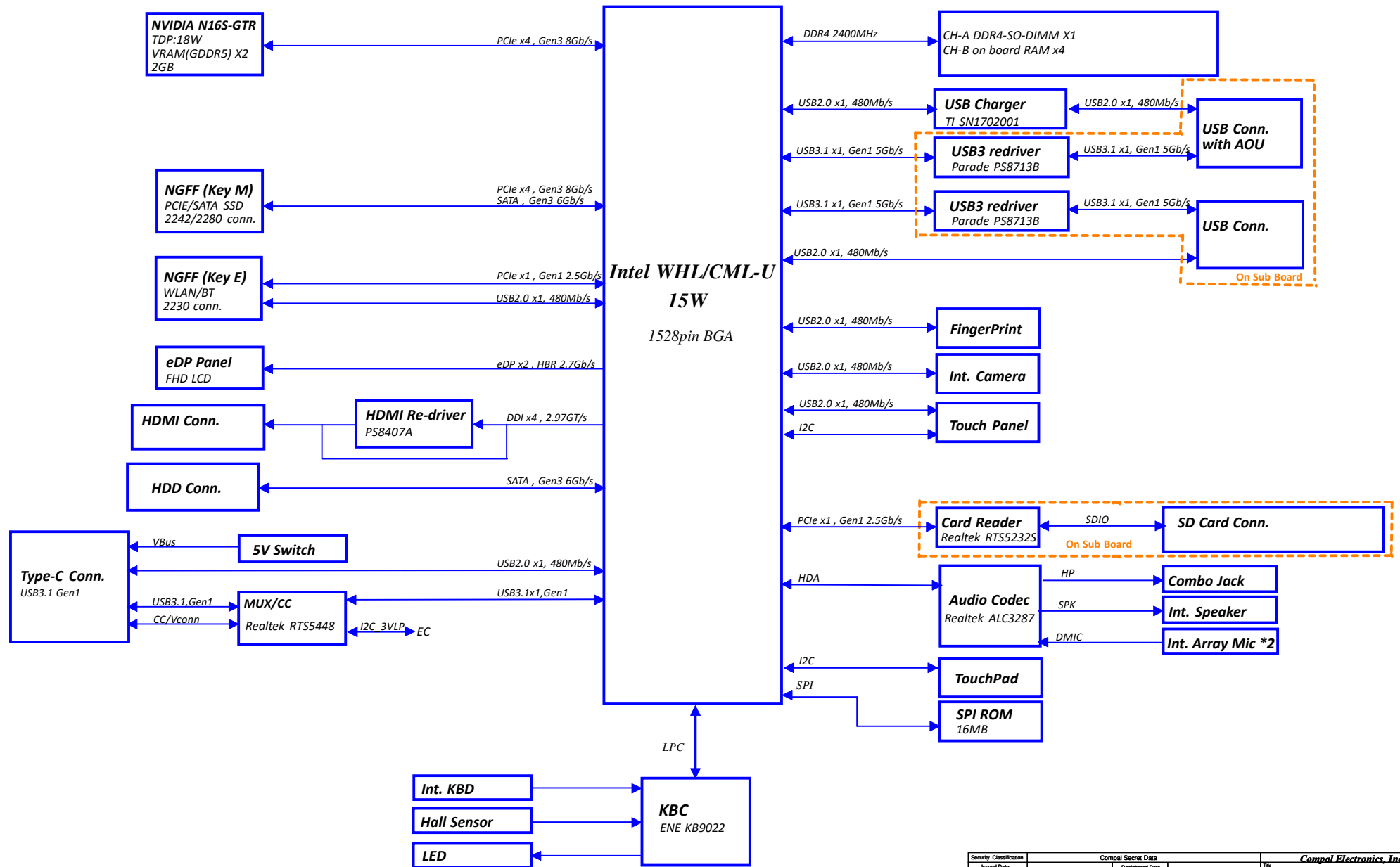
MX110 (23x23mm)

2019-06-24

LA-H104P

REV : 1 . 0

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title Cover Page		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-H104P	1.0
				Date:	Tuesday, June 25, 2019	Sheet 1 of 53



## Voltage Rails

power plane	B+	+5VALW +3VALW +1.8VALW +1.05VALW	+1.2V +2.5V	+5VS +3VS +VCCPLL_OC +1.05VS_VCCSTG +VCC_CORE +VCC_GT +VCC_SA +1.05V_VCCST +1.05VS_VCCIO +1.8VS +0.6VS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

## BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
HDMI Logo	45@
Touch Screen	TS@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
Connectors	ME@
Intel CNVi	CNVi@
EMI Category	EMI@
ESD Category	FP_ESD@
RF Category	ESD@
Test Point	RF@
Keyboard BackLight	TP@
	KBL@
Project select	S540@
	S340@
	C340@
	S340_14@
	S340_15@
GPU select	N17S_G1@
	N17S_G0@
	N16V@
	N16S@
	N16@
	N17@
	MD@
Memory Down select	NO_MD@
MIC select	Array_MIC@
	Single_MIC@
TypeC 20V_PRTCT	20V_PRTCT@
HDMI Level-Shifter	LS@
Un-Mount HDMI Level-Shifter	NO_LS@

## USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

## USB 3.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	
5	
6	

## PCIe Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	DGPU
7	2	
8	3	
9	1	CardReader
10	0	
11		NGFF WLAN+BT
12	0	
13	3	
14	2	
15	1	SSD
16	0	

## SATA Port Table

Port	External SATA Port
0	
1A	HDD
1B	SSD1

## EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x 16h	NCT7718W	1001 100x 98h

## PCH SM Bus address GPU SM Bus address

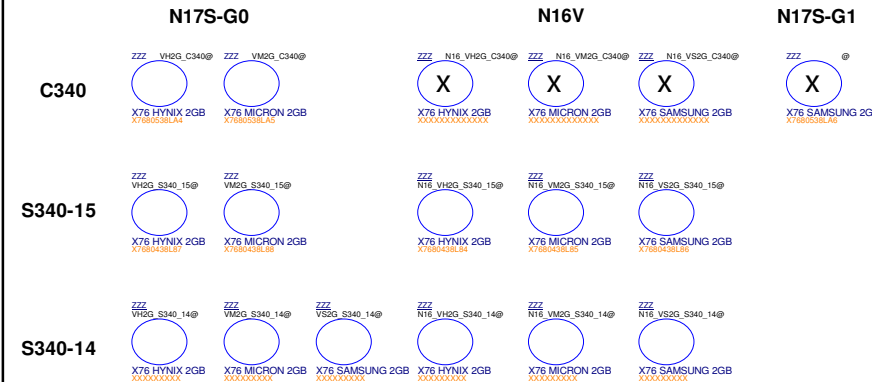
Device	Address	Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h	Internal thermal sensor	1001 111x 9Eh

## SMBUS Control Table

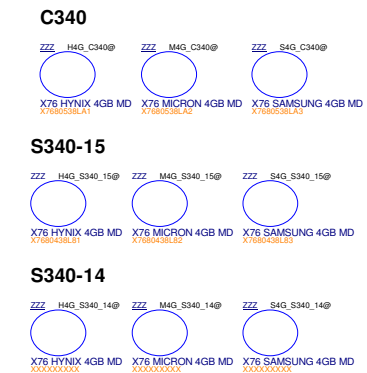
	SOURCE	DGPU	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	G-SENSOR
EC_SMB_CK1 EC_SMB_DA1	NECP388 +3VL	X	+3VALW	+19V_VIN	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	NECP388 +3VS	+3VGS	X	X	+3VS	X	X	X
EC_SMB_CK4 EC_SMB_DA4	NECP388 +3VS	X	X	X	X	X	X	+3VS
SOC_SMBCLK SOC_SMBDATA	SOC +3VS	X	X	X	X	+3VS	X	X
SOC_SML0CLK SOC_SML0DATA	SOC +3VS	X	X	X	+3VS	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

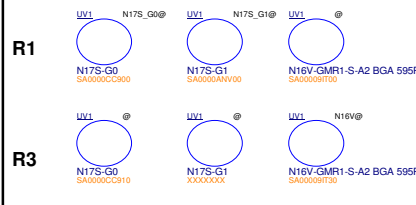
## GDDR5 VRAM \* 2 (total 2GB)



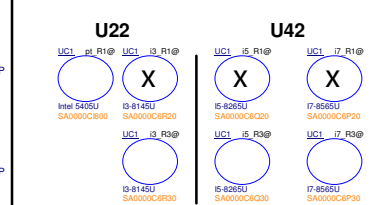
## ON BOARD RAM \* 4 (total 4GB)



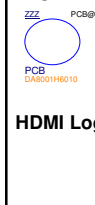
## GPU



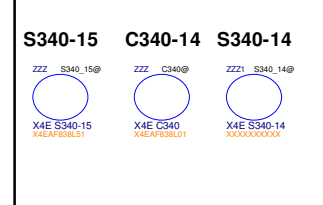
## WHL CPU



## PCB



## X4E



Security Classification	Compal Secret Data	Title	
Issued Date	2018/04/09	Deciphered Date	2019/04/09
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Notes List	
Date: Tuesday, June 26, 2019		Rev 1.0	

## AAXOS Schematic | LA-C071PR01\_1026A.DS1



G3→S0

S0→S3/DS3

S3/DS3→S0

S0→S5

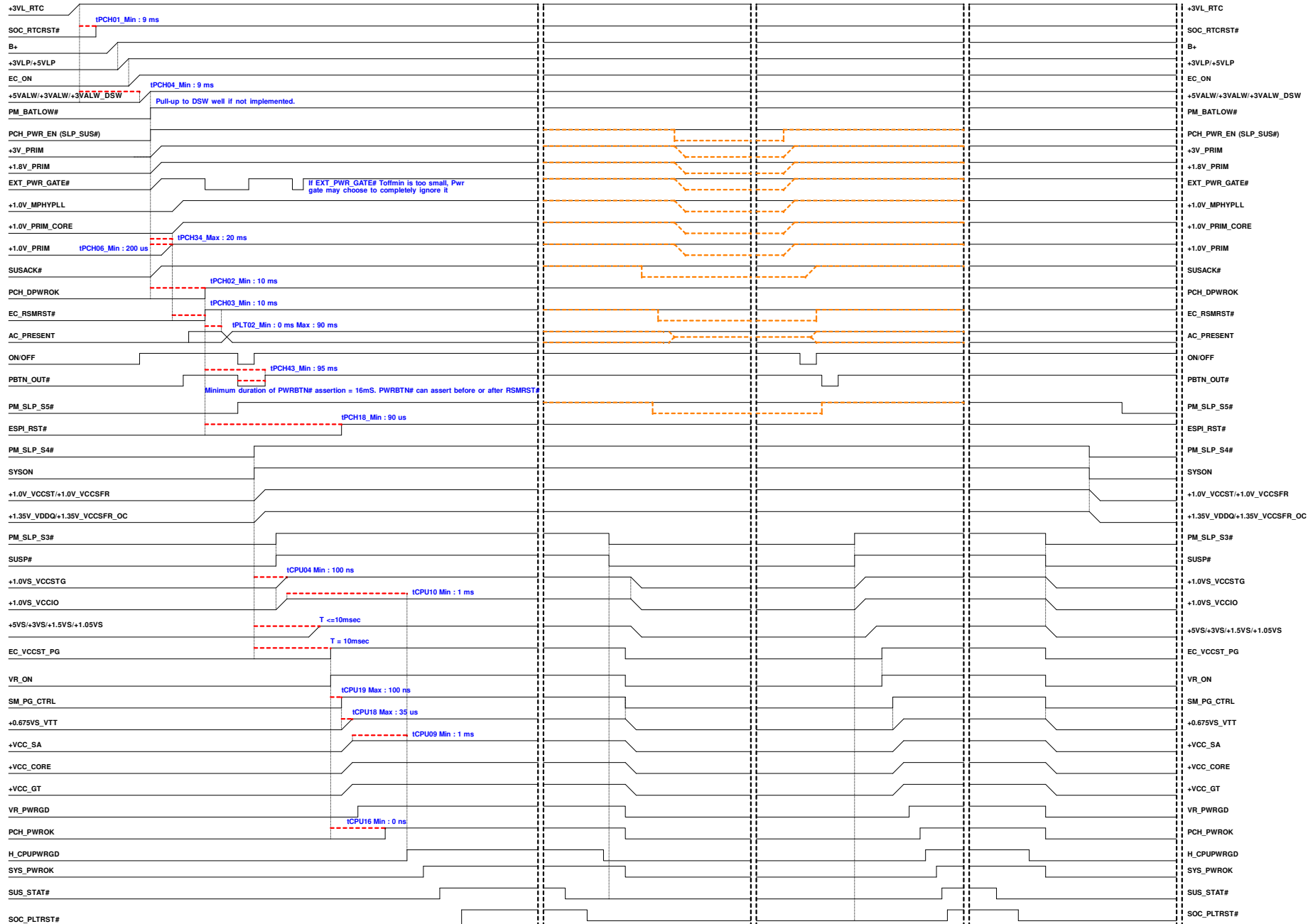
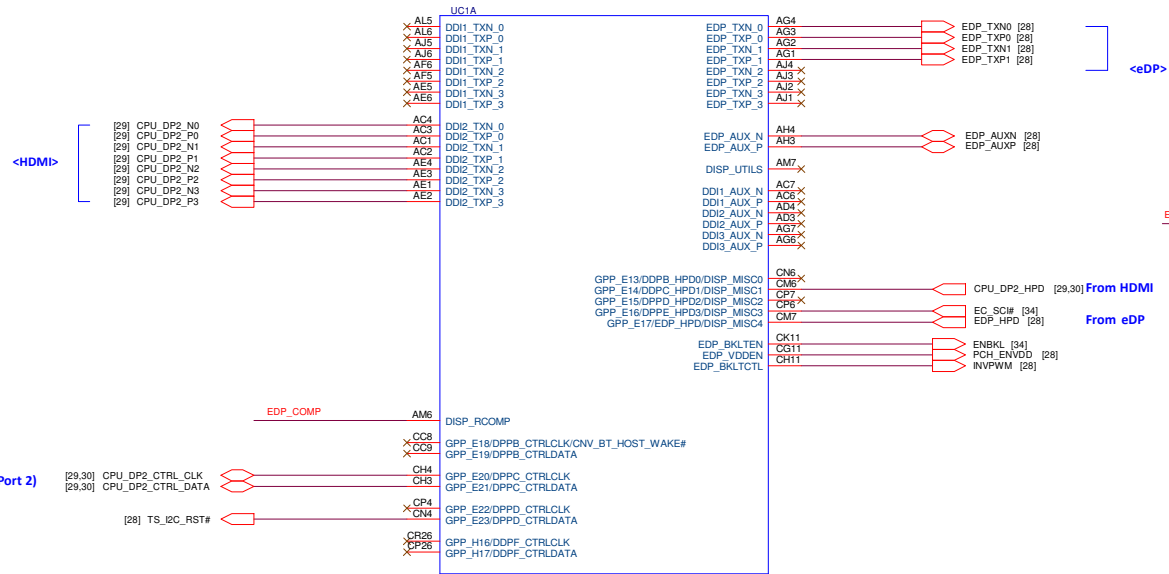


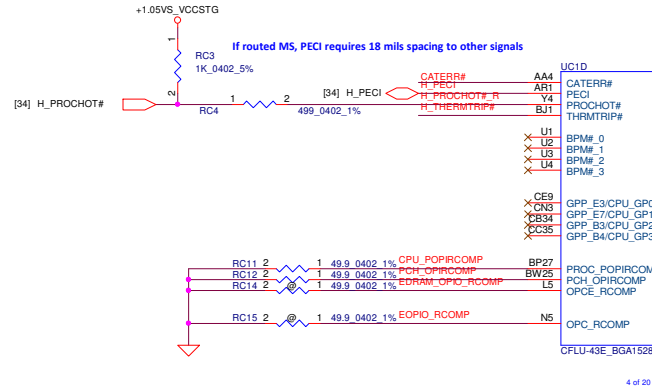
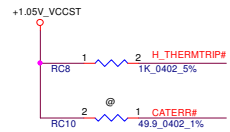
Table 5-13. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 3	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	
Port 4	DDPF_CTRLDATA	Pull up to 3.3 V with 2.2-k ohm $\pm 5\%$ resistor	

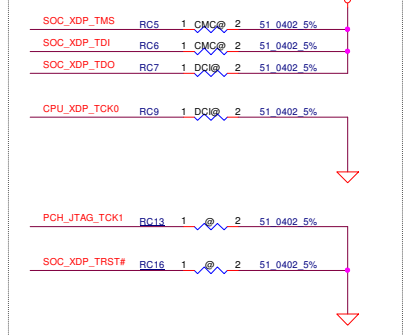
#### < Compensation PU For eDP >



#### HDMI DDC (Port 2)



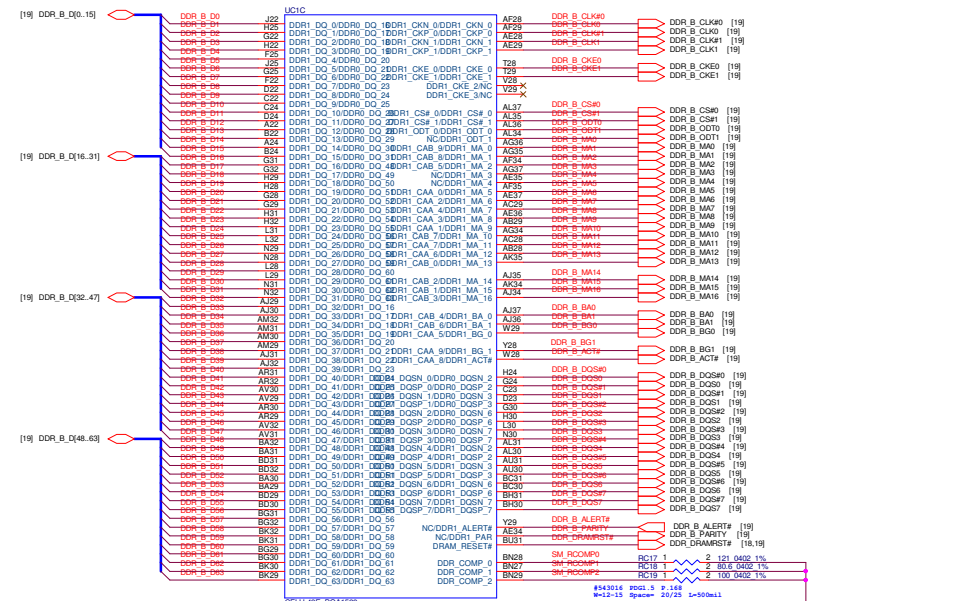
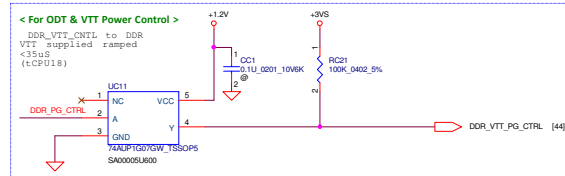
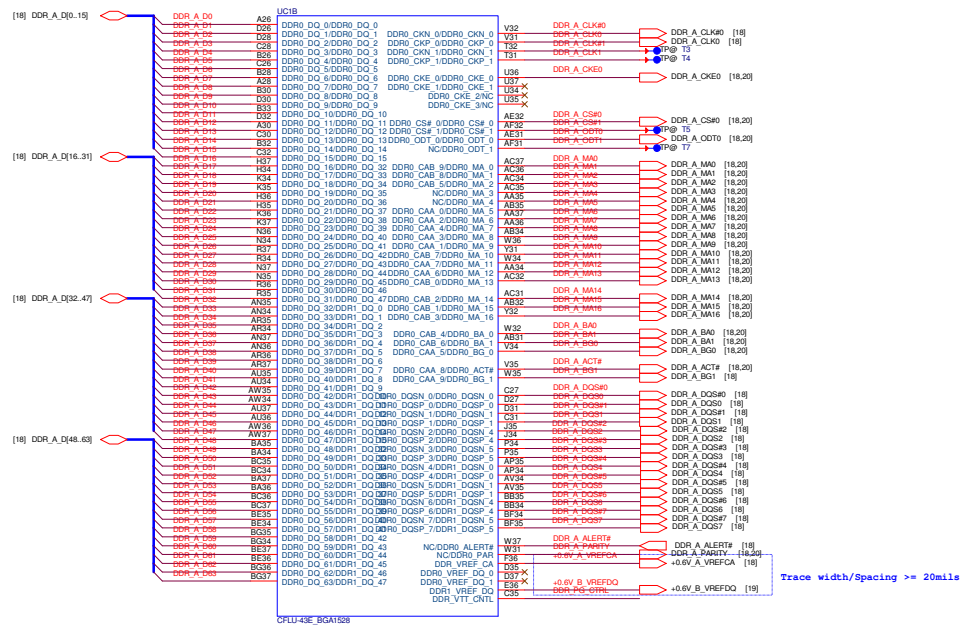
#### < PU/PD for CMC Debug >



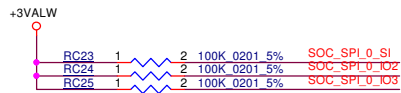
teknisi-indonesia.com

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2018/04/09				Deciphered Date			
2018/04/09				2019/04/09				Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(1/12)DDI.EDP.MISC.CMC				Rev			
Date: Tuesday, June 25, 2019				Sheet 6 of 53				Customer			
				LA-H104P				Rev 1.0			

# Interleaved Memory



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	WHL-U/2122DDR4	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND UNCLASSIFIED INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, WITHOUT PERMISSION IN WRITING FROM COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size	Document Number	Rev
			Unit	LA-H104P	1.0
			Date	Tuesday, June 26, 2018	Sheet 7 of 81



**Note:** The internal pull-up is disabled when RSMRST# is asserted (during reset) and only enabled after RSMRST# de-assertion

SML1ALERT#/  
PCHHOT#/GPP\_B23

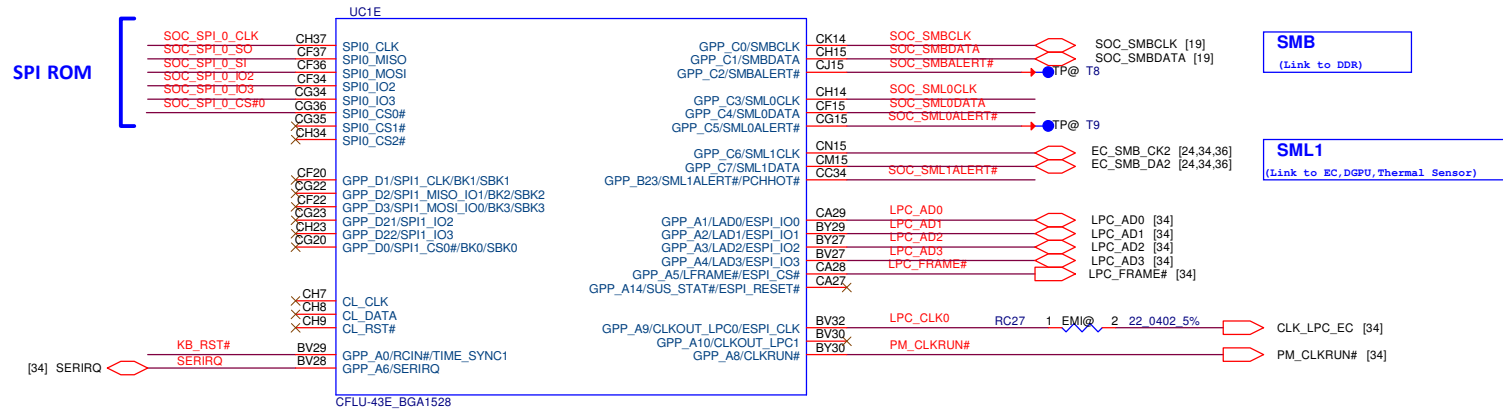
- If USB 3.1 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise.
- If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float.
- If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor

**SML0ALERT# (Internal Pull Down):**

**eSPI or LPC**

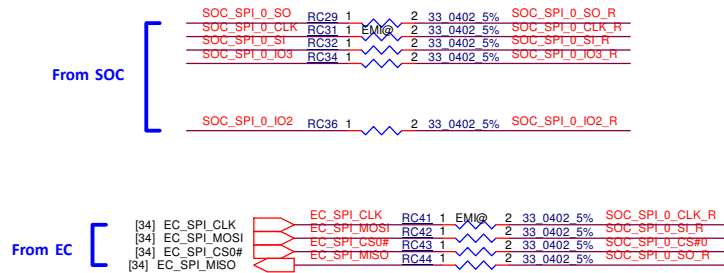
**0 = LPC is selected for EC ==> Default**

**1 = eSPI is selected for EC**

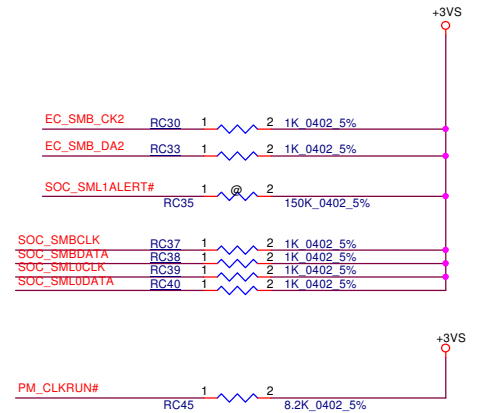
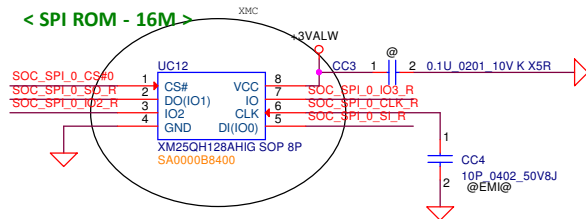


5 of 20

**RPC1, RPC3 and RC30 are close to UC3**



**< SPI ROM - 16M >**

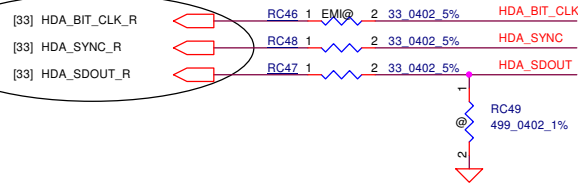


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	WHL-U(3/12)SPI,SMB,LPC,ESPI
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number LA-H104P
				Date	Tuesday, June 25, 2019
				Sheet	8 of 53
				Rev	1.0

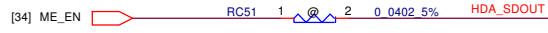


# < HD AUDIO >

5/9 Naming Rule



# < To Enable ME Override >



SPKR (Internal Pull Down):

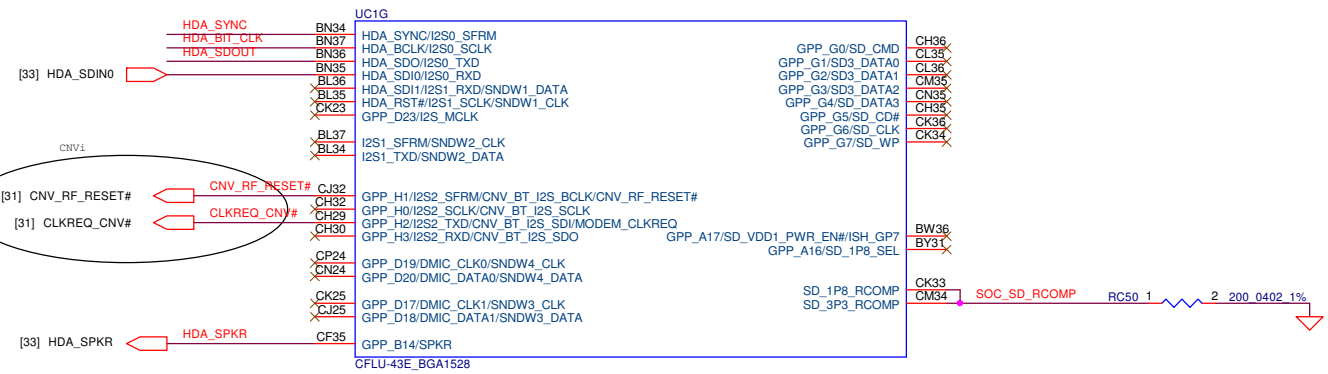
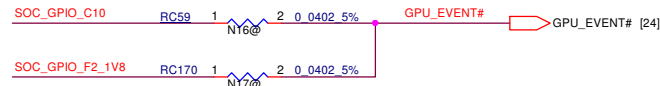
TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

Follow Jefferson Peak schematic check list.

TO DGPU

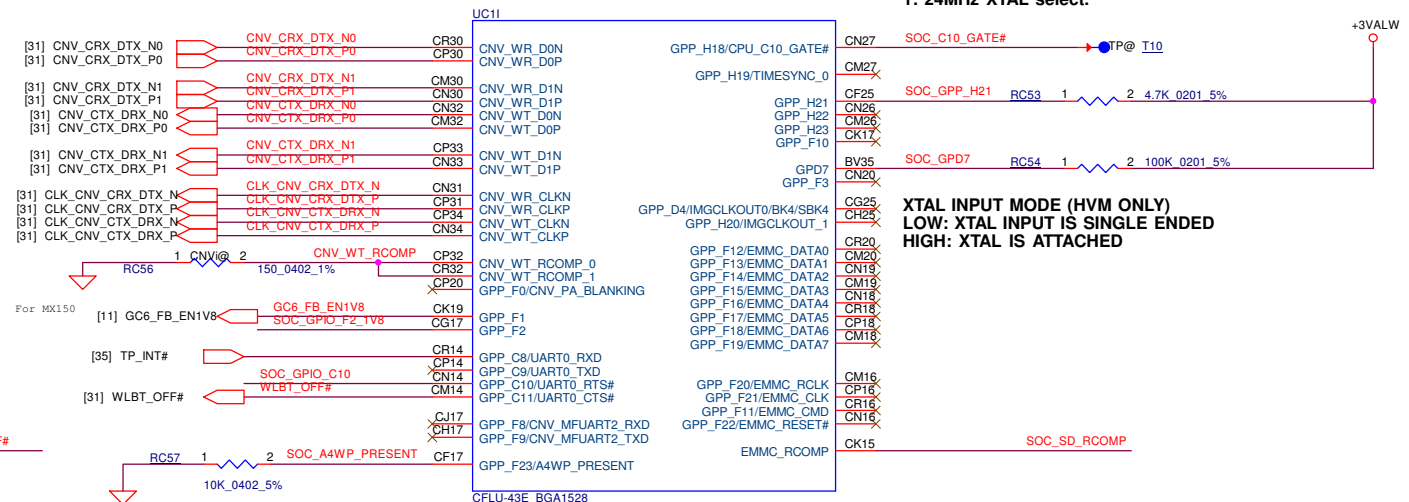


7 of 20

GPP\_H21 XTAL frequency select.

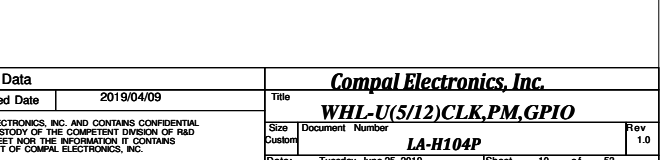
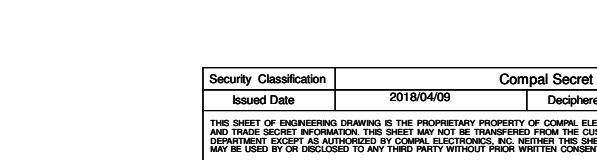
0: 38.4 / 19.2 MHz

1: 24MHz XTAL select.



9 of 20

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2018/04/09		Deciphered Date		2019/04/09		Title			
								WHL-U(4/12)HDA,EMMC,SDIO,CSI2			
Size		Document Number						LA-H104P			
Custom								Rev 1.0			
Date:		Tuesday, June 25, 2019		Sheet		9 of 53					



	Issued Date	
	THIS SHEET OF ENGINEERING DRAWING AND TRADE SECRET INFORMATION. DEPARTMENT EXCEPT AS AUTHORIZED MAY BE USED BY OR DISCLOSED TO	

2 1 Date: Tuesday, June 25, 2019 Sheet 10 of 53

## GPIO\_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

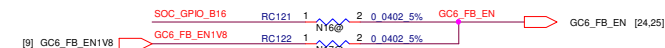
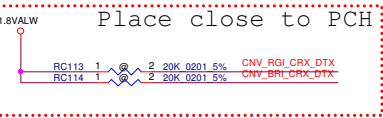
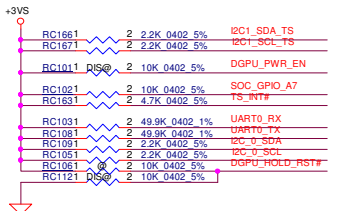
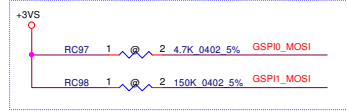
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is used when running ITP/XDP.

## GPIO\_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode



Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

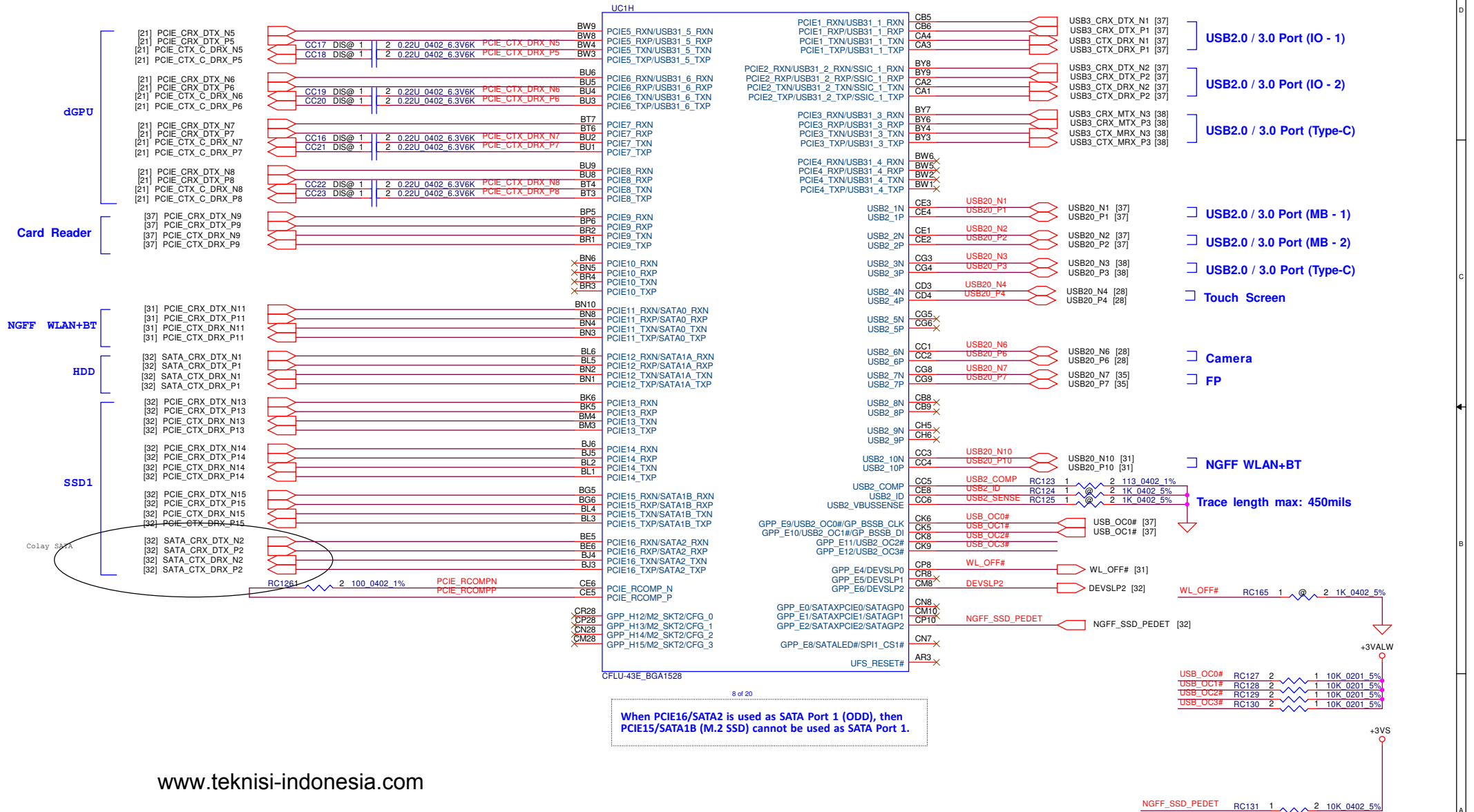
Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		

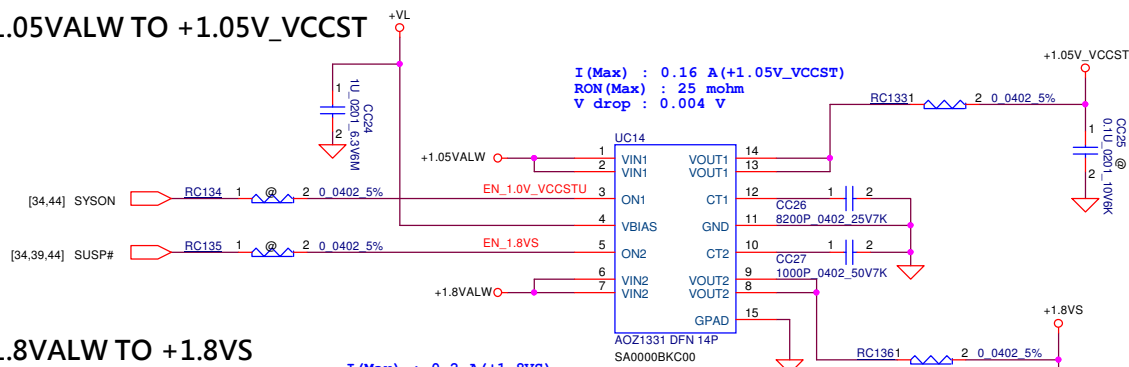
Pin Name	System Pull-up / Pull-down	Schematics Notes	✓
RCINR/GPP_AD	Pull-up to V3.35 with 10 KΩ resistor.	Driven by discrete glue logic or I2O which act as keyboard controller to generate INIT# to the processor.	
PROCPWRGD		This signal is indication of PROCPWRGOOD.	
PIRQA#/GPP_A7	Pull-up to V3.35 with 8.2 KΩ -> 10 KΩ resistor.		



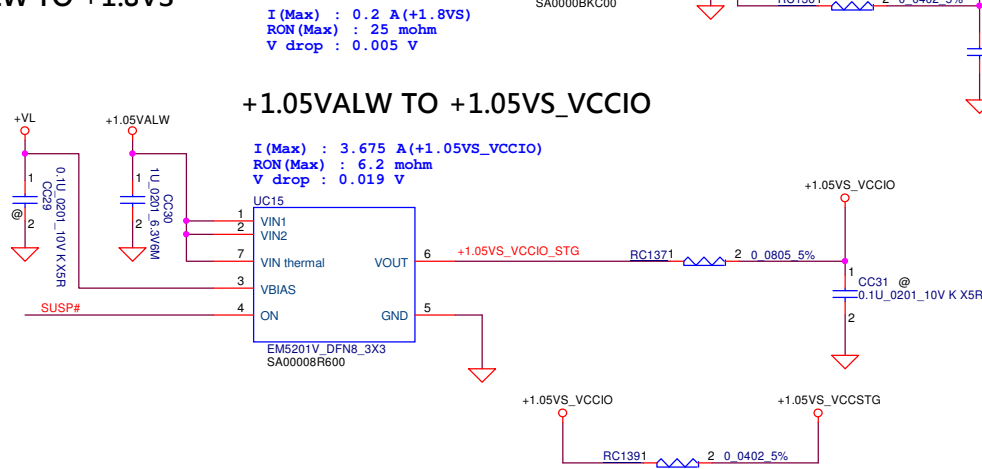
www.teknisi-indonesia.com

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2018/04/09				Deciphered Date			
2018/04/09				2019/04/09				Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(7/12)PCIE,USB,SATA				Size			
								Document Number			
								LA-H104P			
								Date			
								Tuesday, June 25, 2019			
								Sheet			
								12 of 53			
								Rev			
								1.0			

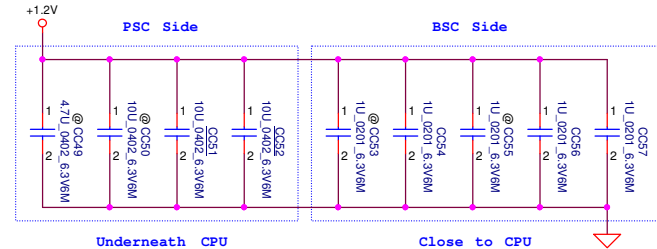
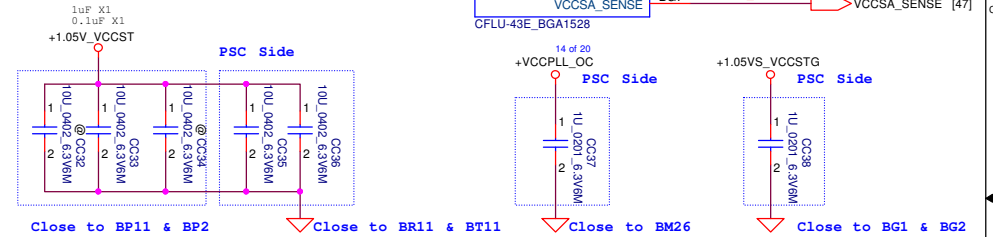
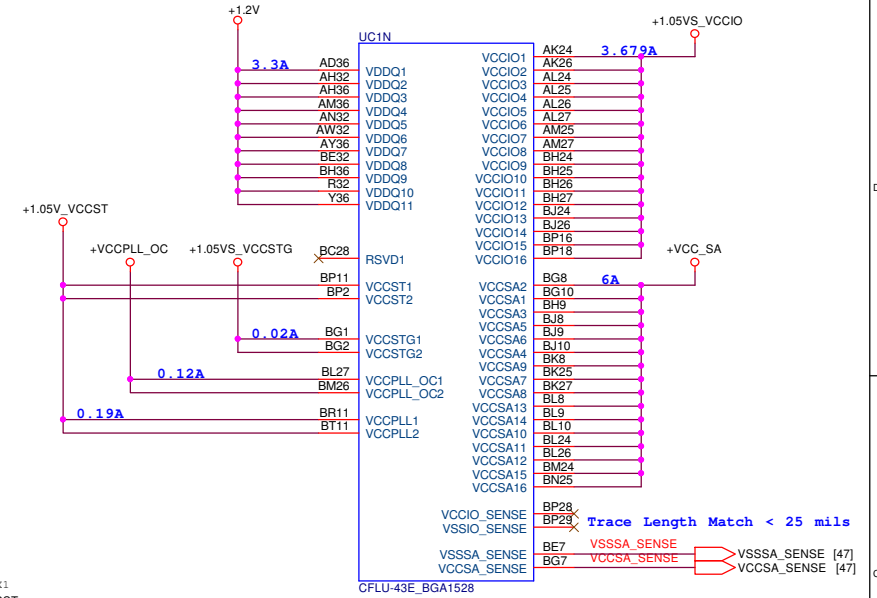
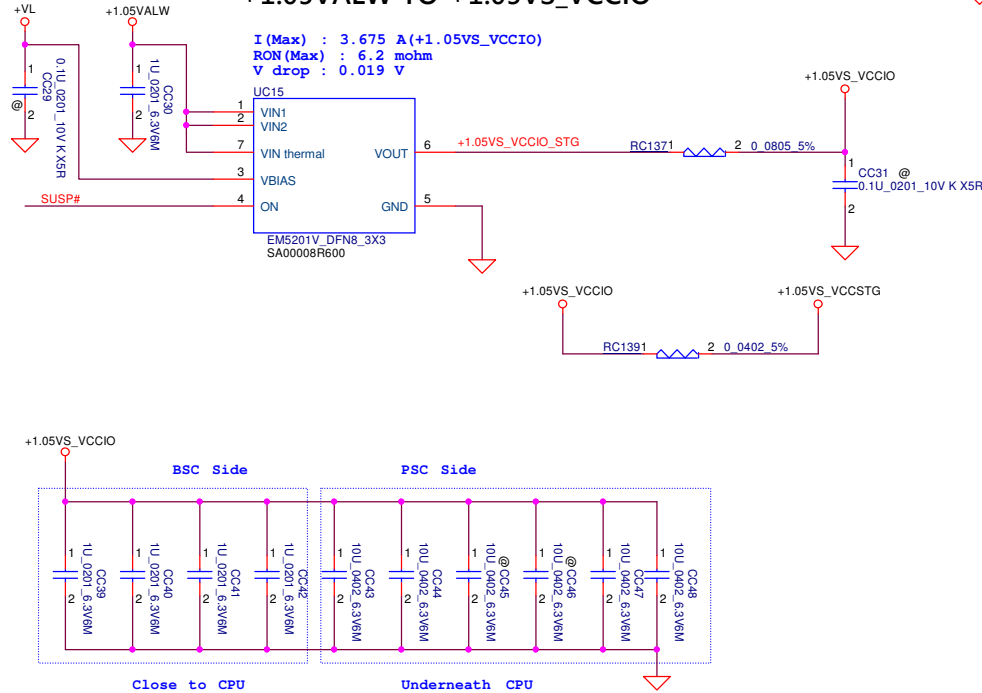
## +1.05VALW TO +1.05V\_VCCST



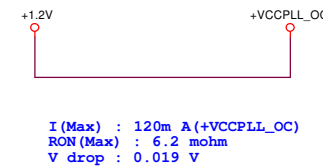
## +1.8VALW TO +1.8VS



## +1.05VALW TO +1.05VS\_VCCIO



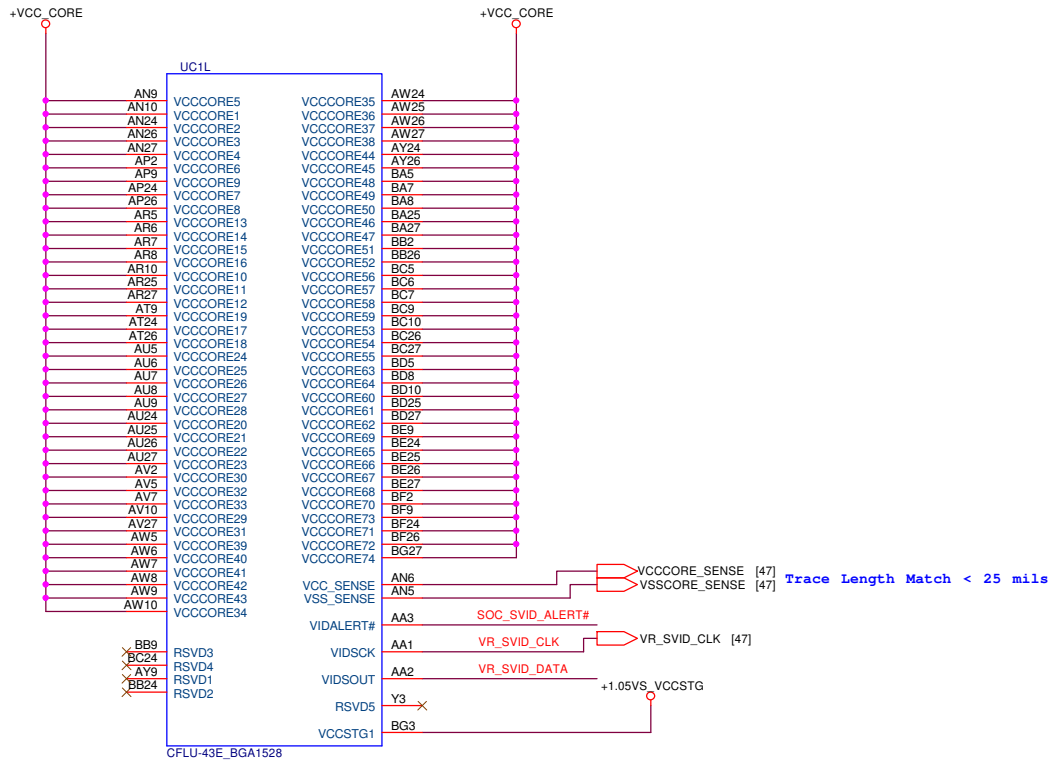
## +1.2V TO +VCCPLL\_OC



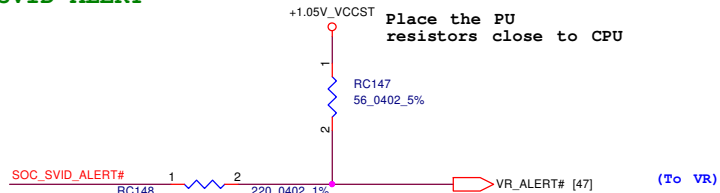
Security Classification		Compal Secret Data		Title	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-H104P
				Date:	Tuesday, June 25, 2019
				Sheet	13 of 53
				Rev	1.0



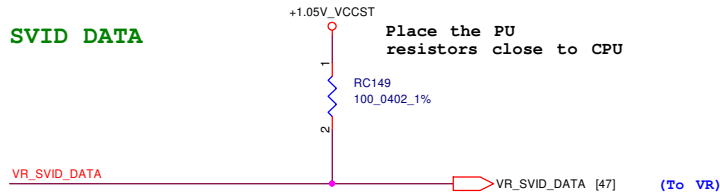




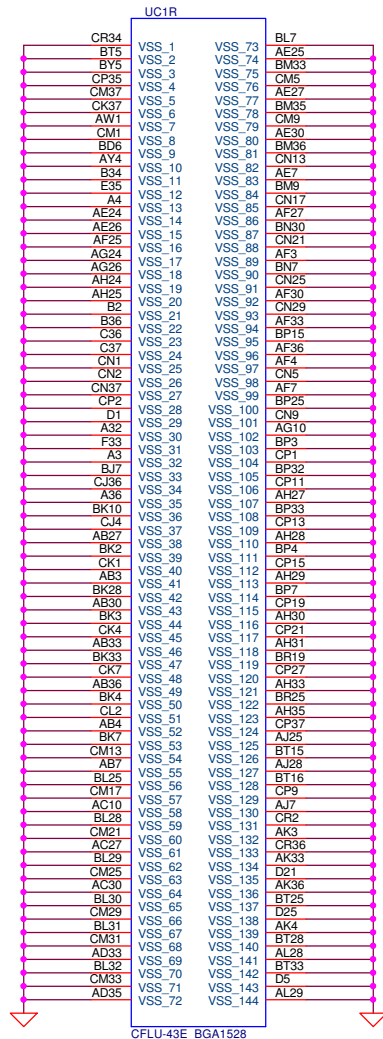
### SVID ALERT



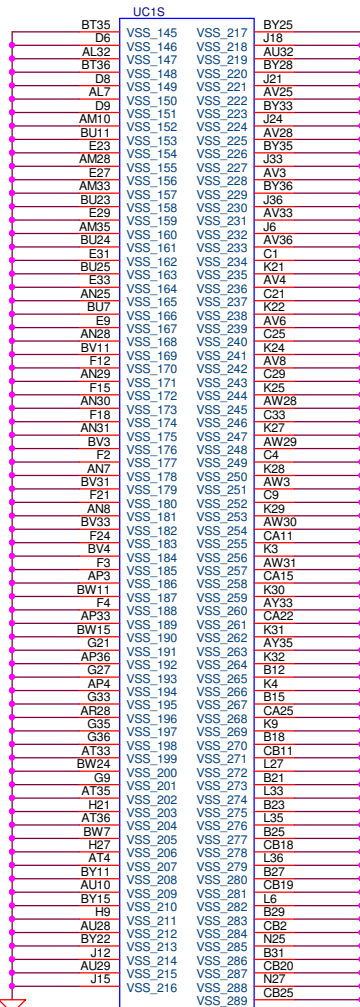
### SVID DATA



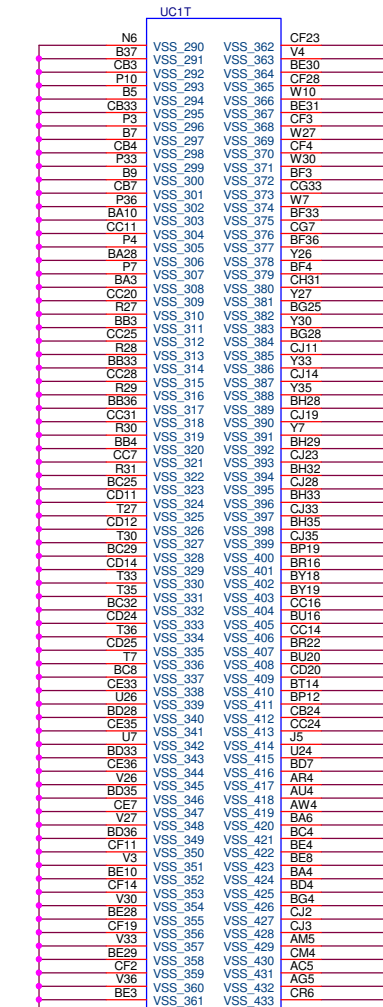
Security Classification		Compal Secret Data		Title	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-H104P
				Date:	Tuesday, June 25, 2019
				Sheet	15 of 53
				Rev	1.0



17 of 20



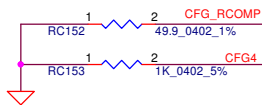
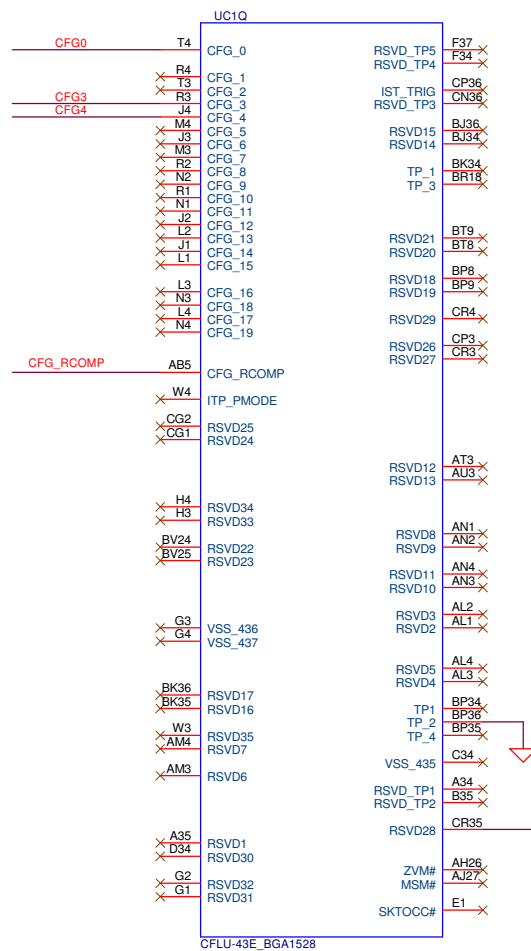
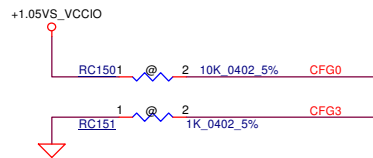
18 of 20



19 of 20

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2018/04/09	Deciphered Date	2019/04/09	Title	
WHL-U(11/12)GND						
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	LA-H104P	1.0
				Date:	Tuesday, June 25, 2019	Sheet





20 of 20

#### DFX Privacy Strap

CFG3

- 1 : Disabled;  
Set DFX disable bit in debug interface MSR
- 0 : Enabled;  
Set DFX enable bit in debug interface MSR

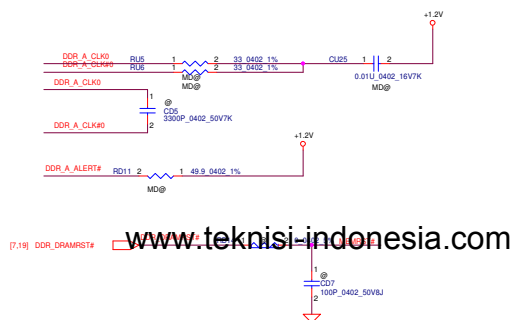
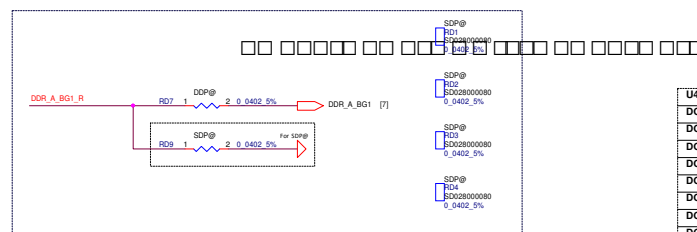
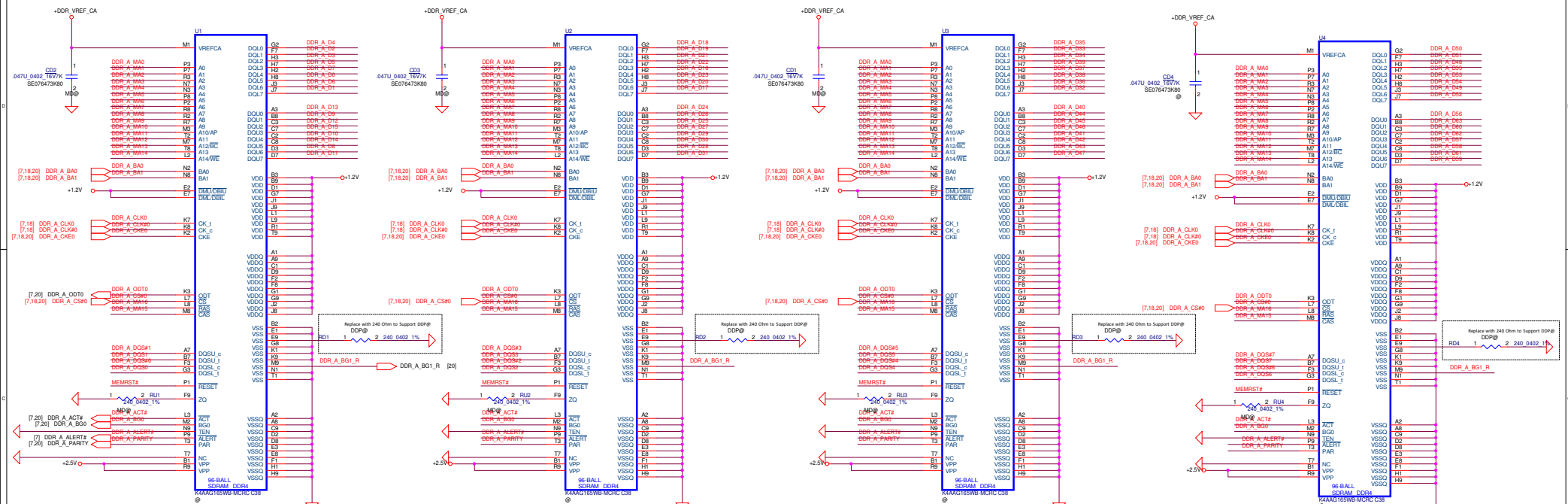
#### Display Port Presence Strap

CFG4

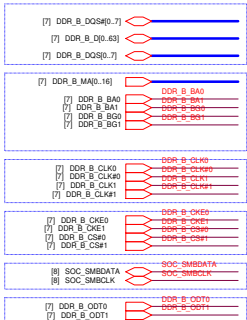
- 1 : Disabled;  
No Physical Display Port at tachedt o E mbedded Dsplay port
- 0 : Enabled;  
An external Display Port device is connected to the Embedded Display Port

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				WHL-U(12/12)CFG,RSVD	
Size Custom	Document Number	LA-H104P		Rev	1.0
Date:	Tuesday, June 25, 2019	Sheet	17 of 53		

## Interleaved Memory

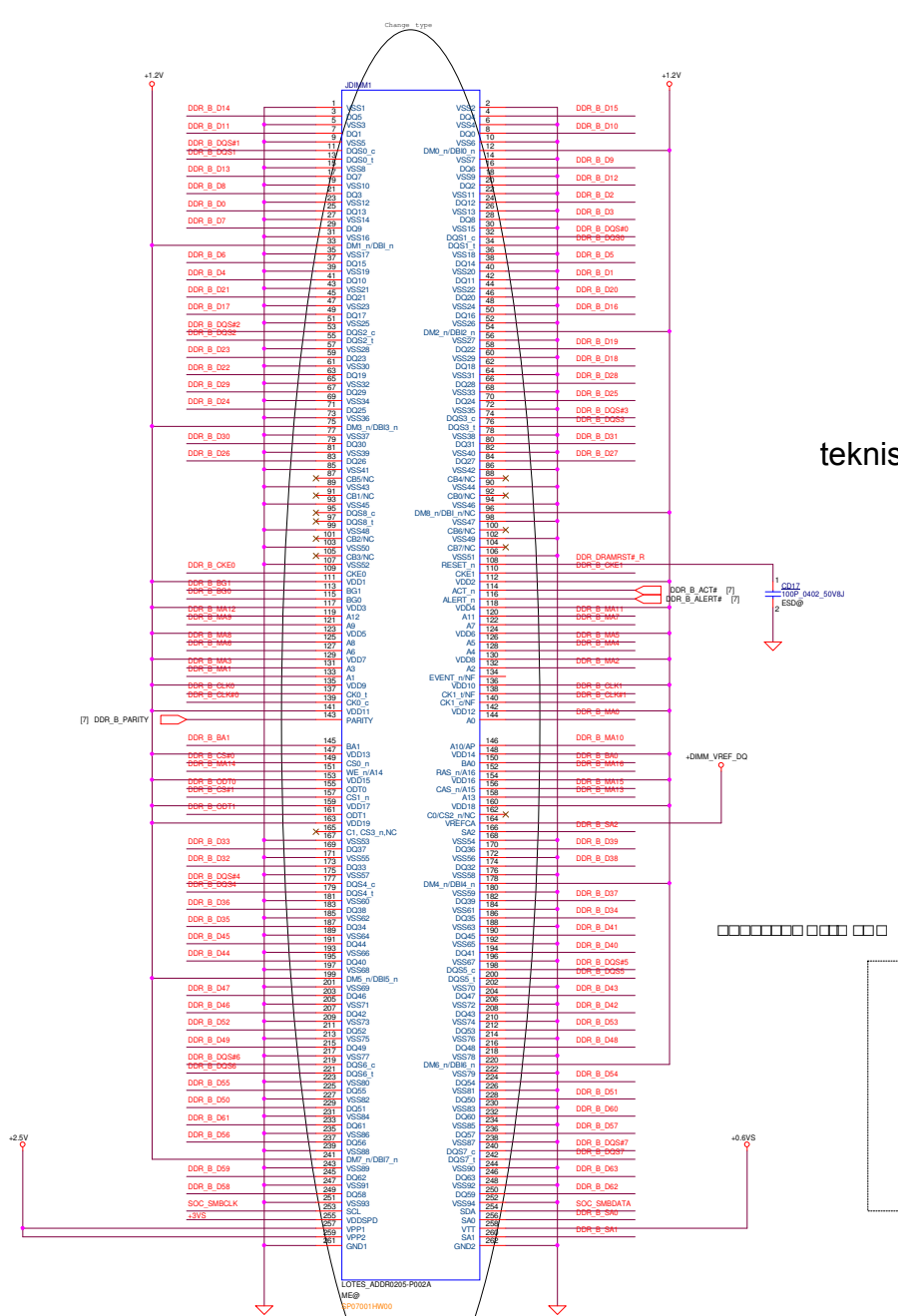
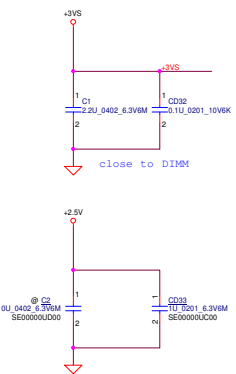
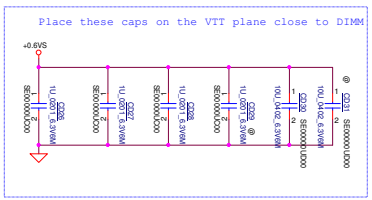
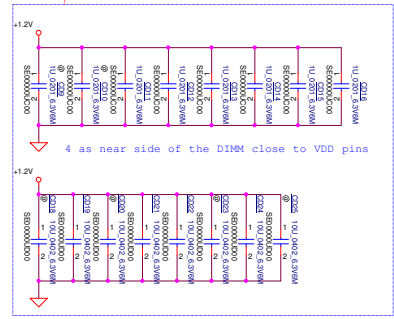


U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

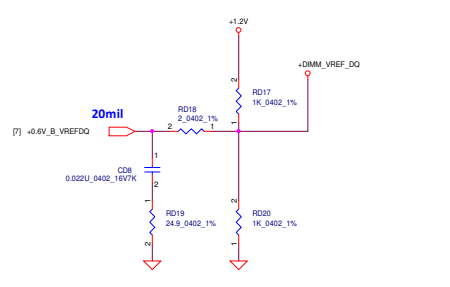


**Layout Note:**  
Place near JDIMM1

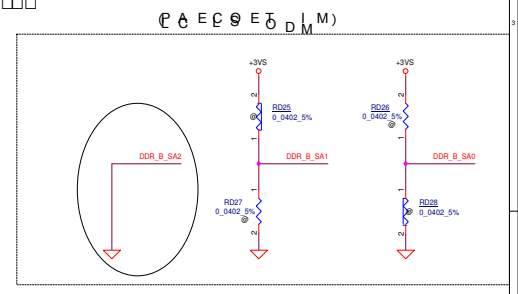
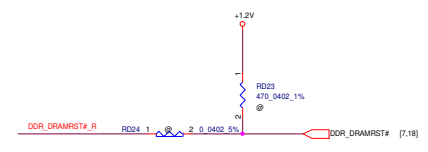
**Note:**  
Check voltage tolerance of VREF\_DQ at the DIMM socket



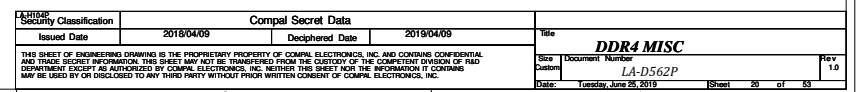
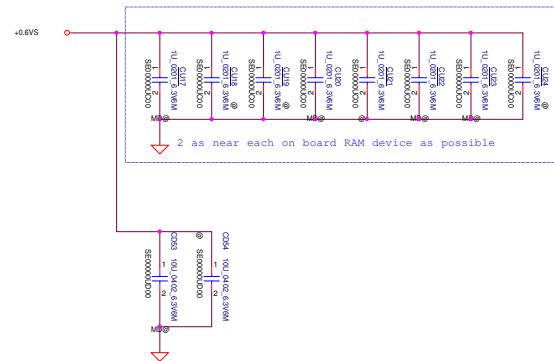
**Standard Type**  
2-3A to 1 DIMMs/channel



teknisi-indonesia.com



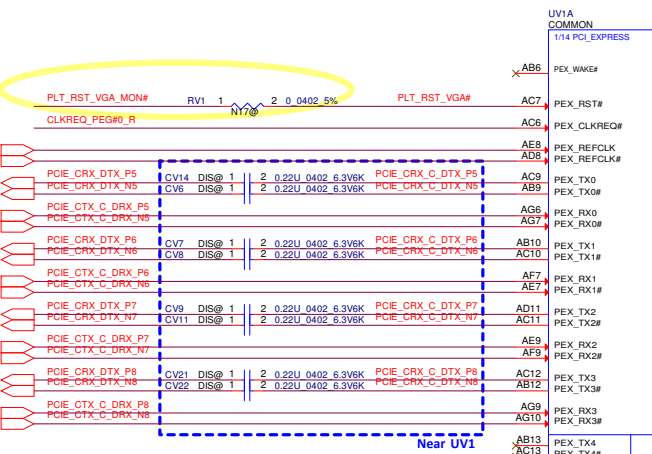
Security Classification		Compal Secret Data		Date		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	File		DDR4 DIMM	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.						Rev	1.0
Size	Document Number	LA-H104P	Rev	1.0	Date:	Tuesday, June 25, 2019	Sheet 19 of 53



# PCIE CLK

# PCIE X4 Bus

- [10] CLK\_PEG\_P0
- [10] CLK\_PEG\_N0
- [12] PCIE\_CRX\_DTX\_P5
- [12] PCIE\_CRX\_DTX\_N5
- [12] PCIE\_CTX\_C\_DRX\_P5
- [12] PCIE\_CTX\_C\_DRX\_N5
- [12] PCIE\_CRX\_DTX\_P6
- [12] PCIE\_CRX\_DTX\_N6
- [12] PCIE\_CTX\_C\_DRX\_P6
- [12] PCIE\_CTX\_C\_DRX\_N6
- [12] PCIE\_CRX\_DTX\_P7
- [12] PCIE\_CRX\_DTX\_N7
- [12] PCIE\_CTX\_C\_DRX\_P7
- [12] PCIE\_CTX\_C\_DRX\_N7
- [12] PCIE\_CRX\_DTX\_P8
- [12] PCIE\_CRX\_DTX\_N8
- [12] PCIE\_CTX\_C\_DRX\_P8
- [12] PCIE\_CTX\_C\_DRX\_N8

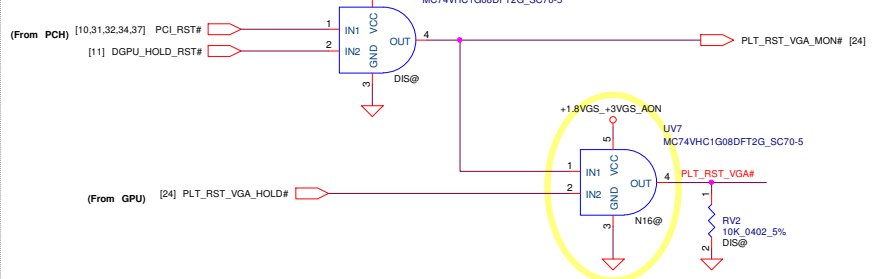


Near UV1

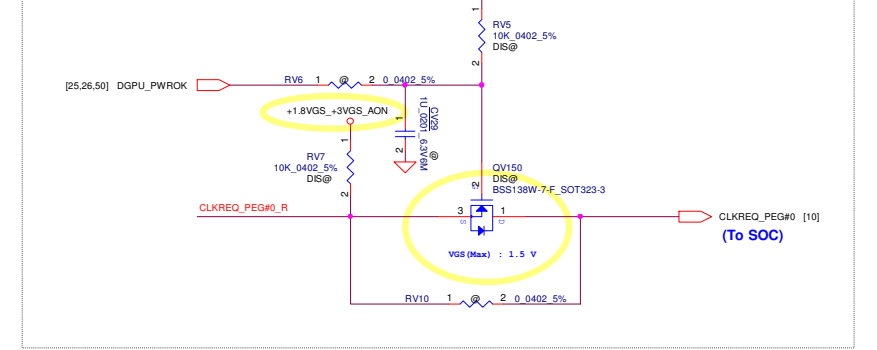
NC FOR GM108

NC FOR GF117/GK208/GM108

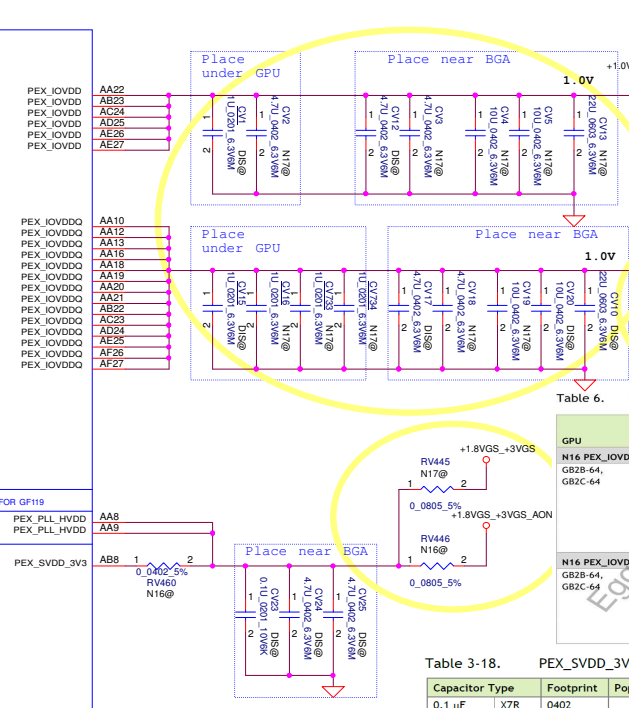
# Reset Control



# CLK\_REQ



(To SOC)



GPU Package Type	Capacitor Type	Footprint	Population	Location
GR2B-64 / GR2C-64	1.0 $\mu$ F X65	0402	1	Under GPU
	4.7 $\mu$ F X65	0603	1	Near GPU
	10 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply
	22 $\mu$ F X5R	0805	1	Midway between GPU and Power Supply

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail				
GR2B-64, GR2C-64	1.0 $\mu$ F X65	0402	1	Under GPU
	4.7 $\mu$ F X65	0603	0	Under GPU
	4.7 $\mu$ F X65	0603	1	Near GPU
	10 $\mu$ F X65	0805	0	Midway between GPU and Power Supply
	22 $\mu$ F X65	0805	0	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail				
GR2B-64, GR2C-64	1.0 $\mu$ F X65	0402	1	Under GPU
	4.7 $\mu$ F X65	0603	1	Near GPU
	10 $\mu$ F X65	0805LP	1	Midway between GPU and Power Supply
	22 $\mu$ F X65	0805LP	1	Midway between GPU and Power Supply

Table 3-18. PEX\_SVDD\_3V3 and PEX\_PLL\_HVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	Near GPU
4.7 $\mu$ F	X5R	0603	Near GPU

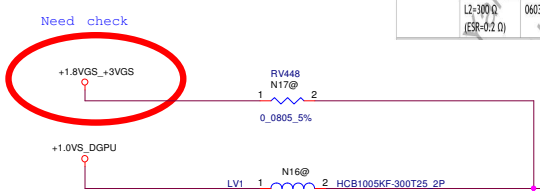
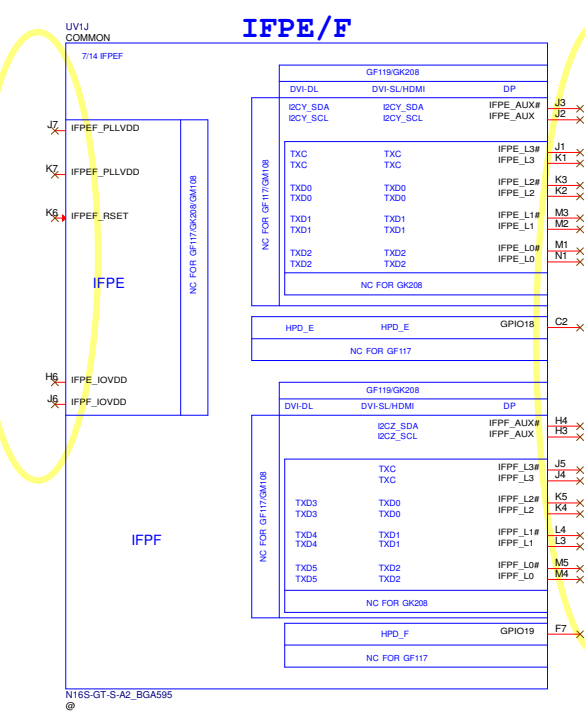
To POWER  
trace width: 16mils  
differential voltage sensing.  
differential signal routing.

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	Location
PEX_PLLVDD Supply Rail				
GR2B-64	0.1 $\mu$ F X7R	0402	1	Under GPU
	1.0 $\mu$ F X5R	0603	1	Near GPU
	4.7 $\mu$ F X5R	0805	1	Near GPU
PEX_SVDD_3V3 Supply Rail				
GR2B-64	4.7 $\mu$ F X5R	0603	2	Near GPU
PEX_PLL_HVDD Supply Rail				
GR2B-64, GR2C-64	0.1 $\mu$ F X7R	0402	1	Near GPU

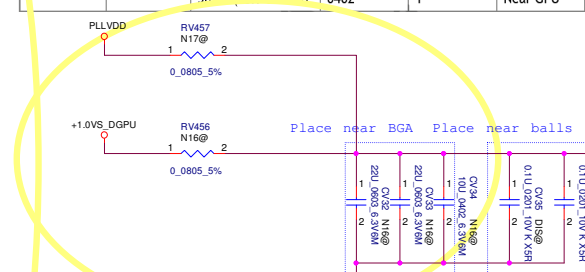
Table 3-17. PEX\_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 $\mu$ F	X7R	0402	1	Under GPU
1.0 $\mu$ F	X5R	0603	1	Near GPU
4.7 $\mu$ F	X5R	0805	1	Near GPU



GPU	Type	Footprint	Population		Location	
			N16	N17		
PLLVD0 (N17: X5, PLLVD0) Supply Rail						
GR28-64, GR2C-64	0.1 $\mu$ F	X7R	0402	1	Under GPU	
	22 $\mu$ F	X5R	0805	0	Near GPU	
Bead Type						
	L2=30 $\Omega$ (ESR=0.05 $\Omega$ )		0402	1	0	Near GPU
SP_PLLVD0 and VID_PLLVD0 Combined Supply Rails						
GR28-64, GR2C-64	0.1 $\mu$ F	X7R	0402	2	Under GPU	
	10 $\mu$ F	X5R	0603	1	0	Near GPU
	47 $\mu$ F	X5R	0805	0	0	Near GPU
Bead Type						
	L2=300 $\Omega$ (ESR=0.2 $\Omega$ )		0603	1	0	Near GPU

GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVD	0.1 $\mu$ F	X7R	0402	1	Under GPU
		22 $\mu$ F	X5R	0805	1	Near GPU
		Bead Type				
		30 $\Omega$ (50B-0.05 $\Omega$ )		0402	1	Near GPU



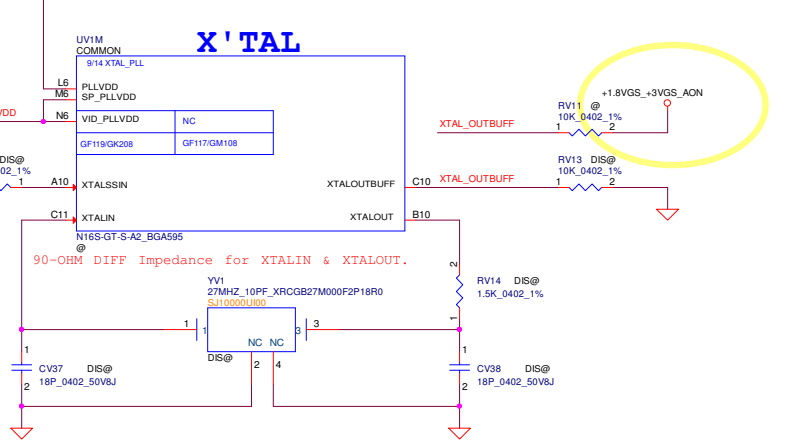
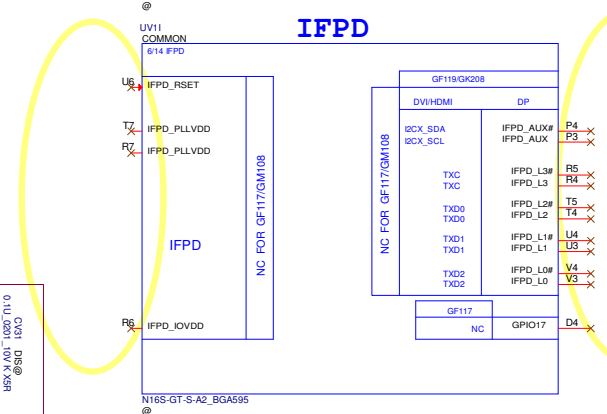
GPU Package	PLL RLLs	Capacitor Type	Footprint	Population	Location
GB2-64	SP_PLLVDD	0.1 $\mu$ F X7R	0402	1 per ball	Under GPU
GB2B-64	(+ VID_PLLVDD) <sup>1</sup>	10 $\mu$ F X5R	0603	1	Near GPU
GB4B-128		47 $\mu$ F X5R	0805	1	Near GPU
GB3B-256		Bead Type			
		300 $\Omega$ (ESR=0.2 $\Omega$ )	0603	1	Near GPU

**Note:**

1. SP\_PLLVDD and VID\_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 X 768 with a 240 Hz

Note:

1. SP\_PLLVDD and VID\_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	<b><u>NV(2/5)-IFP ABCDEF DAC XTAL</u></b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				<b><u>LA-H104P</u></b>	
				Date:	Tuesday, June 25, 2019
				Sheet	22 of 53

# GPU\_Decoupling CAPs @ Power Page

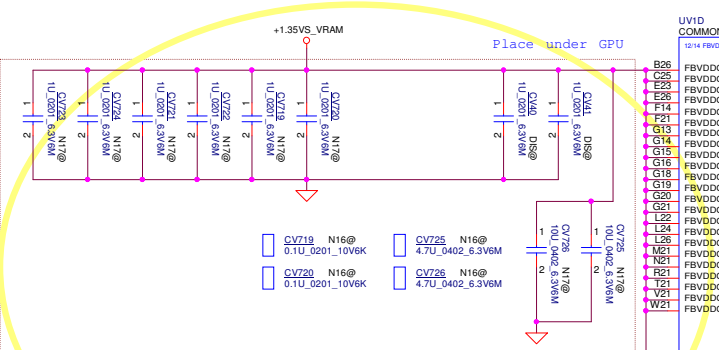
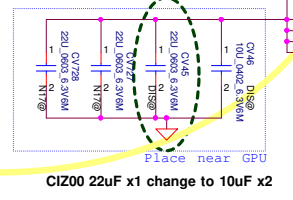
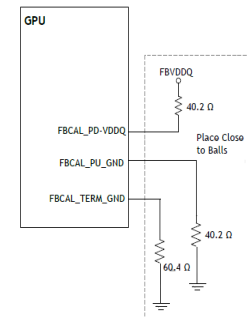
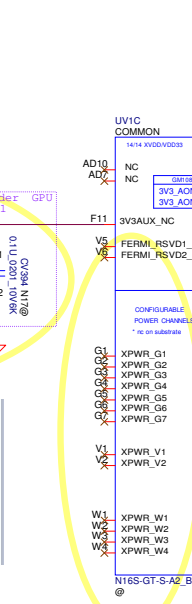
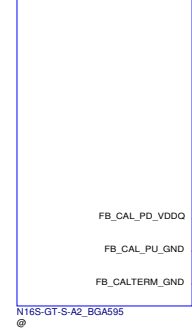
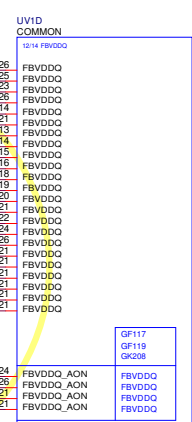


Table 4. Frame Buffer Core and IO Decoupling and Filtering

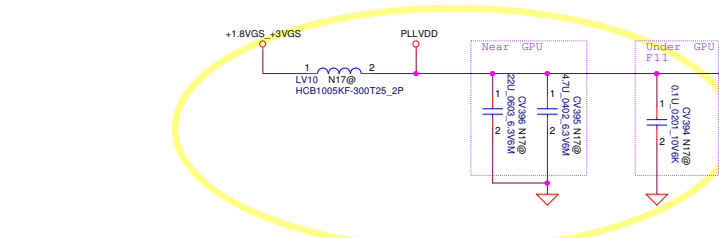
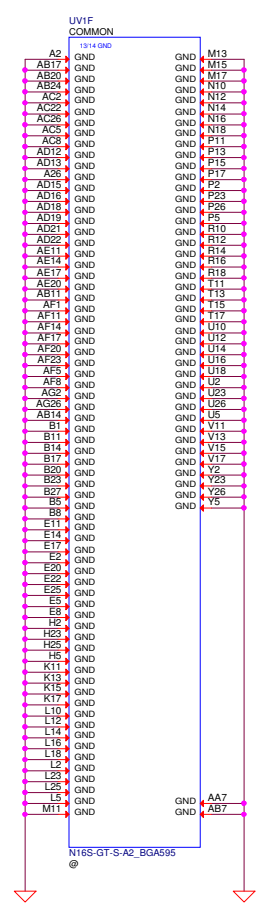
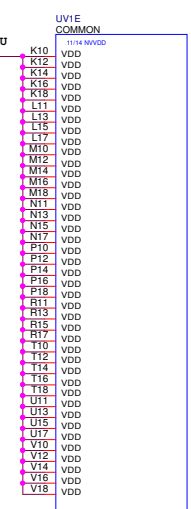
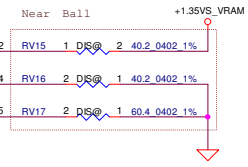
GPU Type	Capacitor Type	Footprint	Population	N16	N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 $\mu$ F	X7R 0402	2	0	0	Under GPU
	1 $\mu$ F	X7R 0603	2	8	0	Under GPU
	4.7 $\mu$ F	X6S 0603	2	0	0	Under GPU
	10 $\mu$ F	X6S 0603	0	2	0	Under GPU
	10 $\mu$ F	X6S 0603	1	1	1	Near GPU
	22 $\mu$ F	X6S 0603W	1	3	0	Near GPU



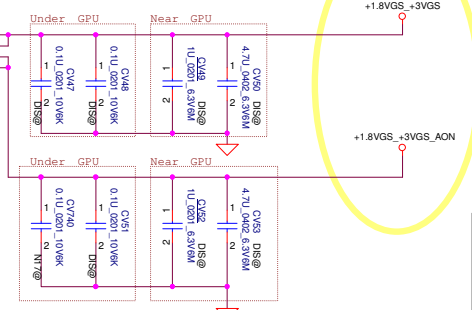
C1Z00 22uF x1 change to 10uF x2



Note: Use only 1% resistors for driver calibration



NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 $\mu$ F	X7R	0402	N/A	1	Under GPU
	4.7 $\mu$ F	X6S	0603	N/A	1	Near GPU
	22 $\mu$ F	X6S	0805	N/A	1	Near GPU
Bead Type						
	L=30 $\Omega$ (ESR=0.010 $\Omega$ )		0603	N/A	1	Near GPU

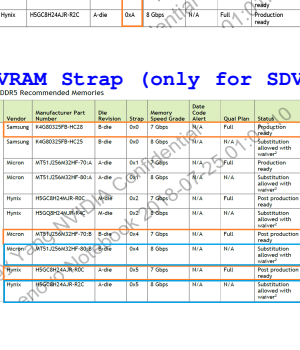
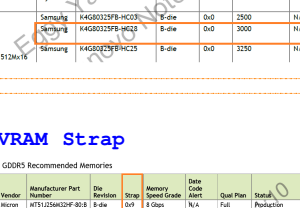
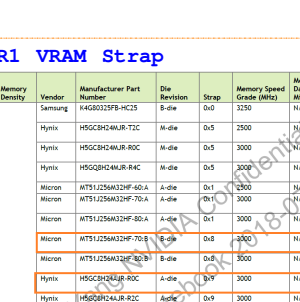
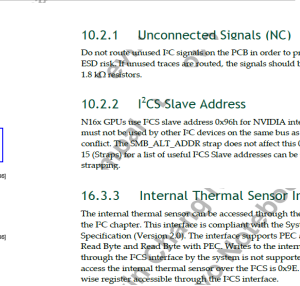
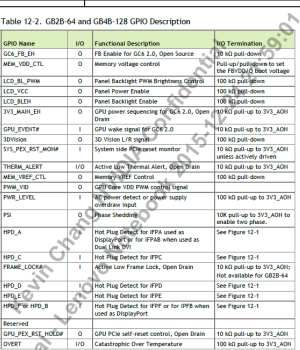






































\*\* XPWR pins are configurable.  
These pins are not connected on the substrate.  
Therefore, XPWR pins can be assigned as needed,  
to improve Top layer routing, power delivery.

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64	3V3_MAIN	0.1 $\mu$ F	X6S	0402	2	2	Under GPU
GB2B-64		1 $\mu$ F	X5R	0603	1	1	Near GPU
GB4B-128 GB3B-256		4.7 $\mu$ F	X5R	0603	1	1	Near GPU
GB2-64	3V3_AON	0.1 $\mu$ F	X6S	0402	1	1	Under GPU
GB2B-64		1 $\mu$ F	X5R	0603	1	1	Near GPU
GB4B-128 GB3B-256		4.7 $\mu$ F	X5R	0603	1	1	Near GPU

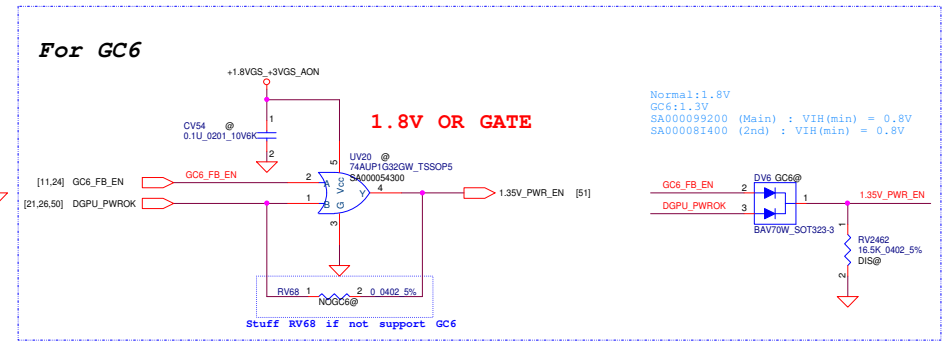
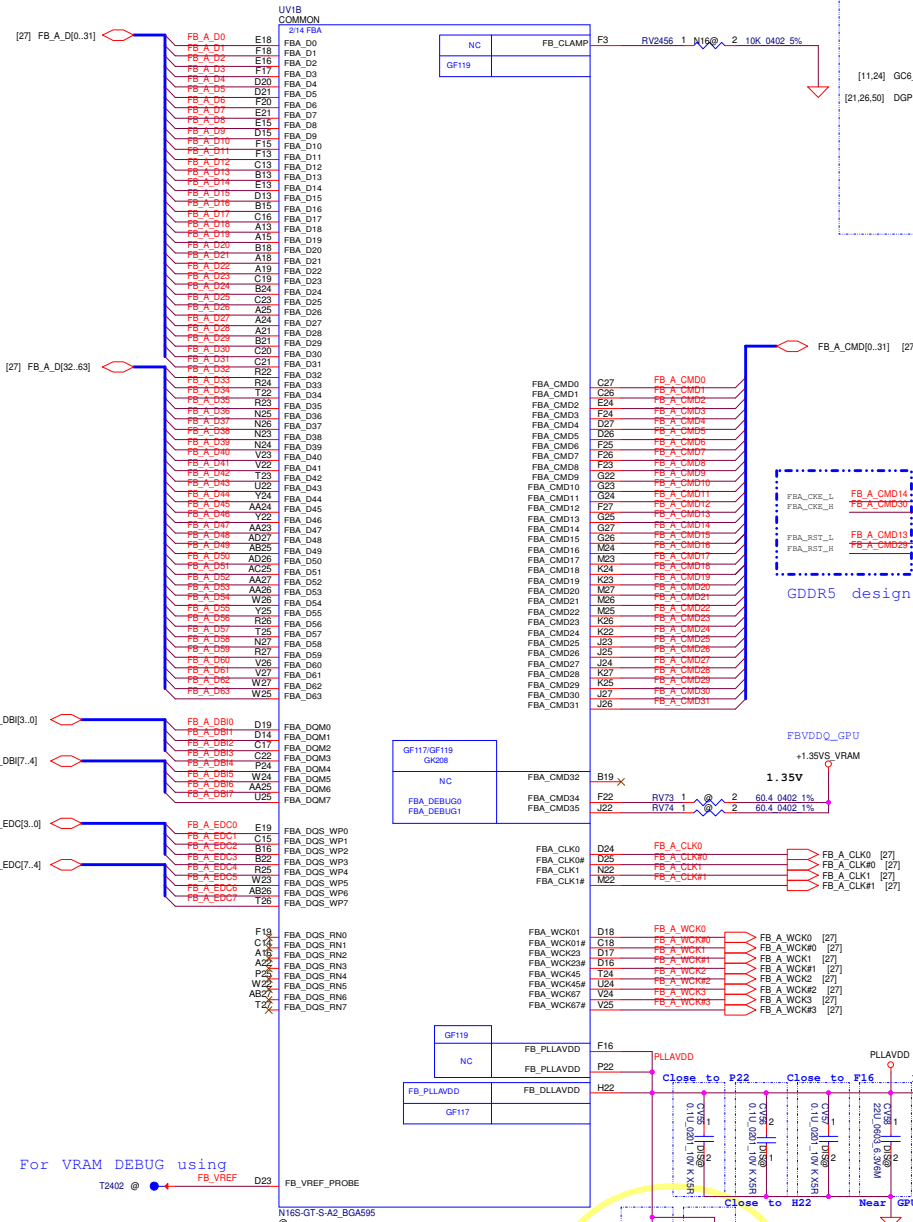
Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.





<p>protect the GPU from outside be pulled down to ground with</p>																																																								
<p>external testing, PC address 0x96h the GPU to avoid address 0x96h address. Refer to Chapter used with SMB_ALT_ADDR</p>																																																								
<p>interface</p>																																																								
<p>the PCS interface as described in from Management Bus (SMBus) and SMBus Timeout as well as thermal sensor registers</p>																																																								
<p>Table 16-1 describes the byte-</p>																																																								
<table> <tr> <th>Memory State Code Minimum</th><th>Status</th></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Post production ready</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Production ready</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Post production ready</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Post production ready</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Production ready</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> <tr> <td>A</td><td>Substitution allowed with value!</td></tr> </table>		Memory State Code Minimum	Status	A	Substitution allowed with value!	A	Post production ready	A	Substitution allowed with value!	A	Substitution allowed with value!	A	Production ready	A	Substitution allowed with value!	A	Substitution allowed with value!	A	Post production ready	A	Substitution allowed with value!	A	Substitution allowed with value!	A	Post production ready	A	Substitution allowed with value!	A	Production ready	A	Substitution allowed with value!	A	Substitution allowed with value!	<table> <tr> <th>RAM_CFG</th><th>ROM_S1</th><th>NOTE</th></tr> <tr> <td><b>S2G</b></td><td></td><td></td></tr> <tr> <td>0x0 4.99K (L)</td><td> R002 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> <tr> <td><b>H2G</b></td><td></td><td></td></tr> <tr> <td>0x8 4.99K (R)</td><td> R003 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> <tr> <td><b>H2G</b></td><td></td><td></td></tr> <tr> <td>0x9 10.0K (R)</td><td> R003 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> </table>		RAM_CFG	ROM_S1	NOTE	<b>S2G</b>			0x0 4.99K (L)	 R002 N17_G0, S2G0P 100K_0402_2%		<b>H2G</b>			0x8 4.99K (R)	 R003 N17_G0, S2G0P 100K_0402_2%		<b>H2G</b>			0x9 10.0K (R)	 R003 N17_G0, S2G0P 100K_0402_2%	
Memory State Code Minimum	Status																																																							
A	Substitution allowed with value!																																																							
A	Post production ready																																																							
A	Substitution allowed with value!																																																							
A	Substitution allowed with value!																																																							
A	Production ready																																																							
A	Substitution allowed with value!																																																							
A	Substitution allowed with value!																																																							
A	Post production ready																																																							
A	Substitution allowed with value!																																																							
A	Substitution allowed with value!																																																							
A	Post production ready																																																							
A	Substitution allowed with value!																																																							
A	Production ready																																																							
A	Substitution allowed with value!																																																							
A	Substitution allowed with value!																																																							
RAM_CFG	ROM_S1	NOTE																																																						
<b>S2G</b>																																																								
0x0 4.99K (L)	 R002 N17_G0, S2G0P 100K_0402_2%																																																							
<b>H2G</b>																																																								
0x8 4.99K (R)	 R003 N17_G0, S2G0P 100K_0402_2%																																																							
<b>H2G</b>																																																								
0x9 10.0K (R)	 R003 N17_G0, S2G0P 100K_0402_2%																																																							
<p>Table 15-2. Resistance Mapping to Hex Values</p> <table> <tr> <th>Resistor Values</th><th>Default for 25°C MAX</th><th>Default for 65°C</th></tr> <tr> <td>4.99 kΩ</td><td>1000</td><td>1000</td></tr> <tr> <td>10.0 kΩ</td><td>1000</td><td>1000</td></tr> <tr> <td>10.0 kΩ</td><td>1000</td><td>0010</td></tr> <tr> <td>20.0 kΩ</td><td>1001</td><td>0011</td></tr> <tr> <td>24.9 kΩ</td><td>1100</td><td>0100</td></tr> <tr> <td>30.1 kΩ</td><td>1101</td><td>0101</td></tr> <tr> <td>34.8 kΩ</td><td>1110</td><td>0110</td></tr> <tr> <td>40.3 kΩ</td><td>1111</td><td>0111</td></tr> </table>		Resistor Values	Default for 25°C MAX	Default for 65°C	4.99 kΩ	1000	1000	10.0 kΩ	1000	1000	10.0 kΩ	1000	0010	20.0 kΩ	1001	0011	24.9 kΩ	1100	0100	30.1 kΩ	1101	0101	34.8 kΩ	1110	0110	40.3 kΩ	1111	0111																												
Resistor Values	Default for 25°C MAX	Default for 65°C																																																						
4.99 kΩ	1000	1000																																																						
10.0 kΩ	1000	1000																																																						
10.0 kΩ	1000	0010																																																						
20.0 kΩ	1001	0011																																																						
24.9 kΩ	1100	0100																																																						
30.1 kΩ	1101	0101																																																						
34.8 kΩ	1110	0110																																																						
40.3 kΩ	1111	0111																																																						
<table> <tr> <th>RAM_CFG</th><th>STRAP2</th><th>STRAP1</th><th>STRAP0</th><th>NOTE</th></tr> <tr> <td>0x9 (LML) <b>H2G</b></td><td> R008 N17_G0, S2G0P 100K_0402_2%</td><td> R001 N17_G0, S2G0P 100K_0402_2%</td><td> R003 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> <tr> <td>0xA (LMS) <b>H2G</b></td><td> R008 N17_G0, S2G0P 100K_0402_2%</td><td> R001 N17_G0, S2G0P 100K_0402_2%</td><td> R004 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> </table>		RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE	0x9 (LML) <b>H2G</b>	 R008 N17_G0, S2G0P 100K_0402_2%	 R001 N17_G0, S2G0P 100K_0402_2%	 R003 N17_G0, S2G0P 100K_0402_2%		0xA (LMS) <b>H2G</b>	 R008 N17_G0, S2G0P 100K_0402_2%	 R001 N17_G0, S2G0P 100K_0402_2%	 R004 N17_G0, S2G0P 100K_0402_2%																																									
RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE																																																				
0x9 (LML) <b>H2G</b>	 R008 N17_G0, S2G0P 100K_0402_2%	 R001 N17_G0, S2G0P 100K_0402_2%	 R003 N17_G0, S2G0P 100K_0402_2%																																																					
0xA (LMS) <b>H2G</b>	 R008 N17_G0, S2G0P 100K_0402_2%	 R001 N17_G0, S2G0P 100K_0402_2%	 R004 N17_G0, S2G0P 100K_0402_2%																																																					
<table> <tr> <th>RAM_CFG</th><th>STRAP2</th><th>STRAP1</th><th>STRAP0</th><th>NOTE</th></tr> <tr> <td>0x0 (LLL) <b>S2G</b></td><td> R002 N17_G0, S2G0P 100K_0402_2%</td><td> R005 N17_G0, S2G0P 100K_0402_2%</td><td> R006 N17_G0, S2G0P 100K_0402_2%</td><td></td></tr> </table>		RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE	0x0 (LLL) <b>S2G</b>	 R002 N17_G0, S2G0P 100K_0402_2%	 R005 N17_G0, S2G0P 100K_0402_2%	 R006 N17_G0, S2G0P 100K_0402_2%																																														
RAM_CFG	STRAP2	STRAP1	STRAP0	NOTE																																																				
0x0 (LLL) <b>S2G</b>	 R002 N17_G0, S2G0P 100K_0402_2%	 R005 N17_G0, S2G0P 100K_0402_2%	 R006 N17_G0, S2G0P 100K_0402_2%																																																					
<p>Table 5.3. RAMCFG</p> <table> <tr> <th>Strap Pins, see Note</th><th>RAMCFG Setting Number</th></tr> <tr> <th>STRAP2</th><th>STRAP1</th><th>STRAP0</th><th>(see Memory NVL for memory configs corresponding to these numbers)</th></tr> <tr> <td>L</td><td>L</td><td>L</td><td>0 (0x0000)</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>1 (0x0001)</td></tr> <tr> <td>L</td><td>M</td><td>L</td><td>2 (0x0002)</td></tr> <tr> <td>L</td><td>M</td><td>M</td><td>3 (0x0003)</td></tr> <tr> <td>L</td><td>L</td><td>L</td><td>4 (0x0004)</td></tr> <tr> <td>M</td><td>L</td><td>M</td><td>5 (0x0005)</td></tr> <tr> <td>M</td><td>M</td><td>M</td><td>6 (0x0006)</td></tr> <tr> <td>M</td><td>M</td><td>L</td><td>7 (0x0007)</td></tr> <tr> <td>L</td><td>L</td><td>M</td><td>8 (0x0008)</td></tr> <tr> <td>L</td><td>M</td><td>M</td><td>9 (0x0009)</td></tr> <tr> <td>L</td><td>M</td><td>L</td><td>10 (0x000A)</td></tr> </table>		Strap Pins, see Note	RAMCFG Setting Number	STRAP2	STRAP1	STRAP0	(see Memory NVL for memory configs corresponding to these numbers)	L	L	L	0 (0x0000)	L	L	L	1 (0x0001)	L	M	L	2 (0x0002)	L	M	M	3 (0x0003)	L	L	L	4 (0x0004)	M	L	M	5 (0x0005)	M	M	M	6 (0x0006)	M	M	L	7 (0x0007)	L	L	M	8 (0x0008)	L	M	M	9 (0x0009)	L	M	L	10 (0x000A)					
Strap Pins, see Note	RAMCFG Setting Number																																																							
STRAP2	STRAP1	STRAP0	(see Memory NVL for memory configs corresponding to these numbers)																																																					
L	L	L	0 (0x0000)																																																					
L	L	L	1 (0x0001)																																																					
L	M	L	2 (0x0002)																																																					
L	M	M	3 (0x0003)																																																					
L	L	L	4 (0x0004)																																																					
M	L	M	5 (0x0005)																																																					
M	M	M	6 (0x0006)																																																					
M	M	L	7 (0x0007)																																																					
L	L	M	8 (0x0008)																																																					
L	M	M	9 (0x0009)																																																					
L	M	L	10 (0x000A)																																																					
<p>Security Classification</p> <p>2018/07/05</p> <p>Compul Secret Data</p> <p>Deciphered Date</p> <p>2018/04/09</p>		<p>Compul Electronics, Inc.</p> <p>NV(45)-GPIO/Strap</p> <p>LA-H104P</p>																																																						





From DG-07158-001\_v05\_secured(NVDIA Spec)

### 7.1.8 CKE\* Signal

Two copies of the clock enable signal (CKE\*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE\* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

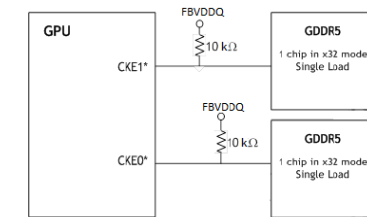


Figure 7-4. Clock Enable (CKE\*) Signal Connection, ×32 Mode

#### 7.1.7.3 RST\* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

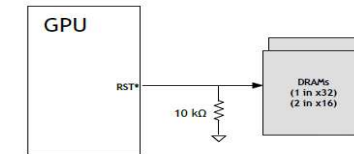


Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GR2-64/	FBx_PLL_AVDD	0.1 μF	X7R	0402	2
GR2B-64	FBx_PLL_AVDD and FBx_DLL_AVDD Combined	22 μF	X5R	0805	1
		Bead Type			
		30 Ω (ESR=0.010 Ω)	0603	1	Near GPU

Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
FB PLL Supply Rail for GDDR5						
GR2B-64,	0.1 μF	X7R	0402	2	4	Under GPU
GR2C-64	22 μF	X65	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

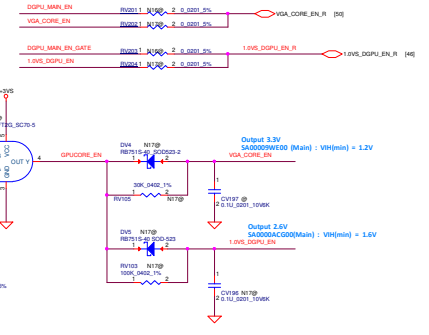
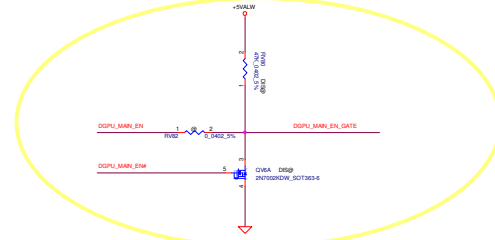
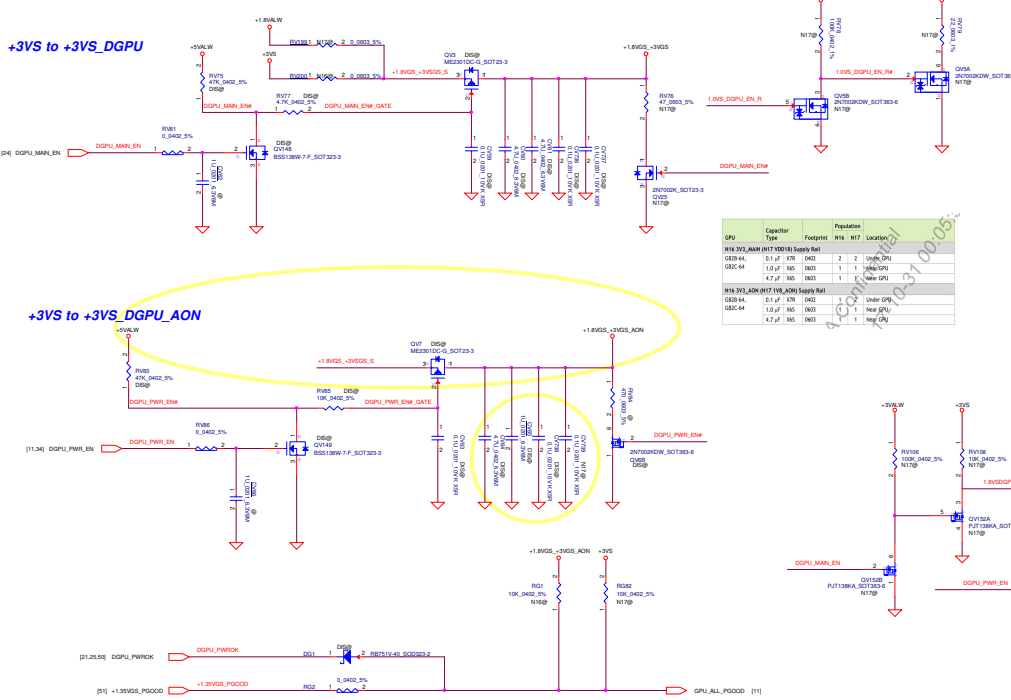


Table 5. EDP-Continuous <sup>3</sup>

Products	VRAM Type	GPU Core		GPU FBIO		FB Total <sup>1, 5</sup>		1.05V Total <sup>2</sup>	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06	
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06	
N165-GTR	GDDR5	26.5	—	2.0	—	4.2	0.80	0.06	
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06	

Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

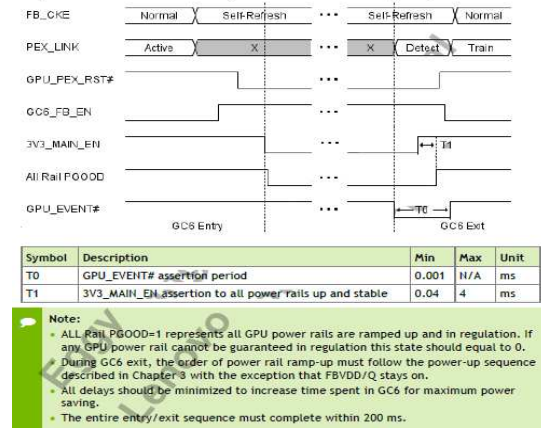


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# deassertion	0.1	5	ms

Note:

- 3.3V includes all rails powered at 3.3V. PEX\_VDD includes all rails that are shared on 1.05V/1.0V.
- The ramp time for any rail must be more than 40  $\mu$ s and is recommended to be less than 2 ms.

## VRAM Memory Partition A

Table 7-4. GDDR5 Mode H Mapping

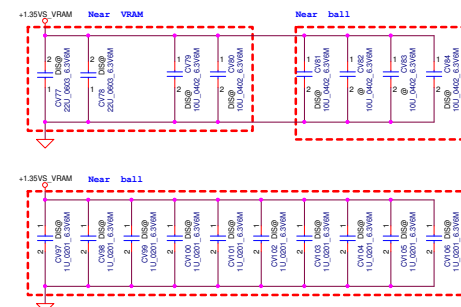
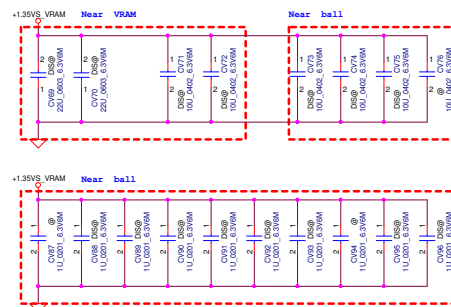
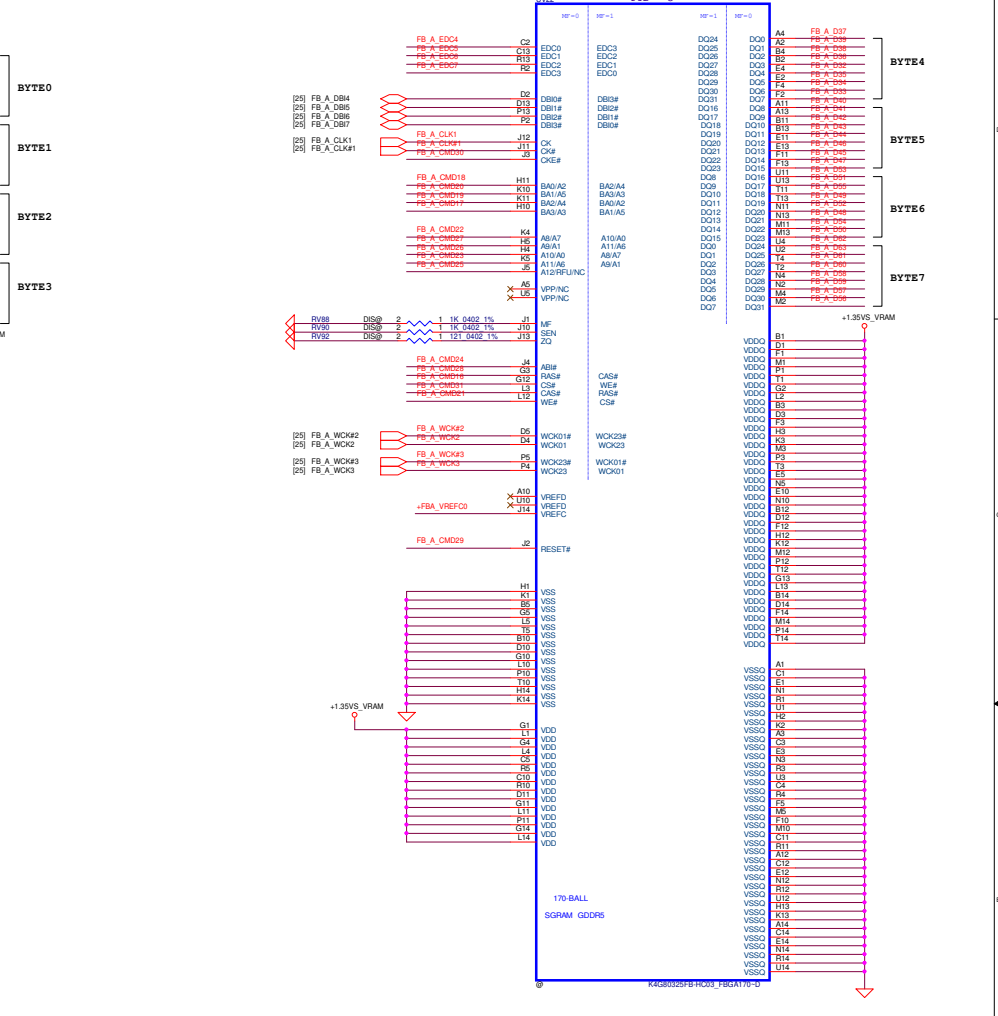
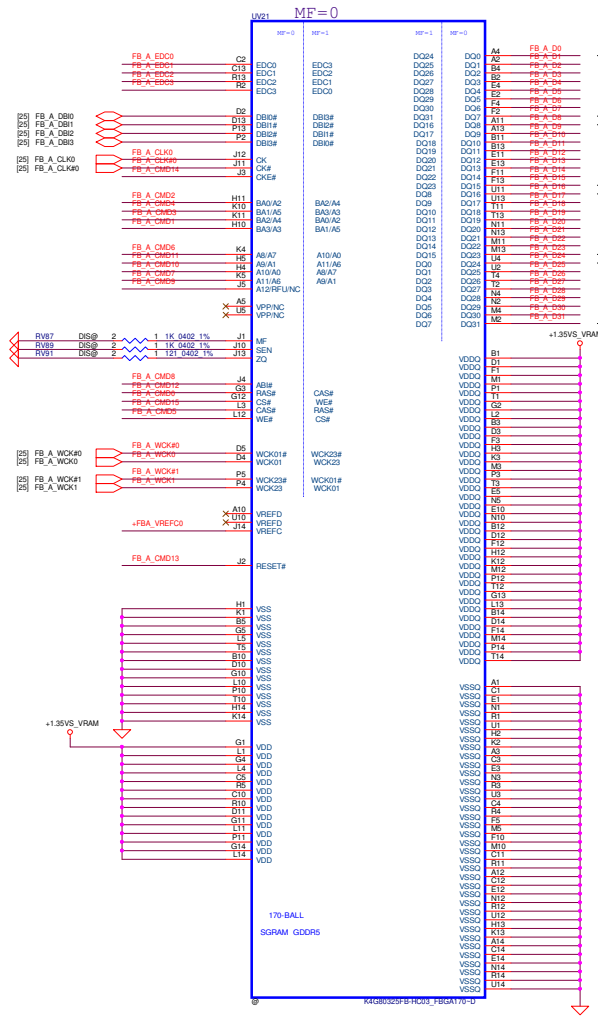
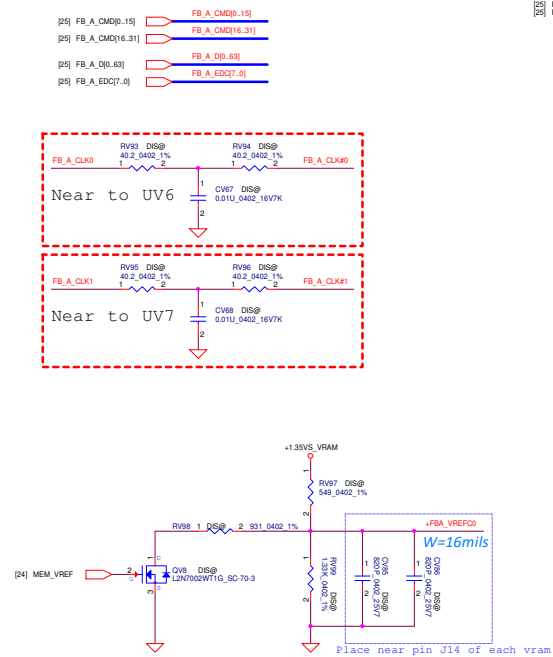
GB2-64, GB28-64, GB48-128	Channel 0 0.31	GB2-64, GB28-64, GB48-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CA5*	CMD31	CA5*
GB2-64, GB28-64, GB48-128	Channel 0 & 1		
CMD32	Hot_user		
CMD33*	Hot_user		
CMD34	DEBUG0*		
CMD35	DEBUG1*		

Notes:

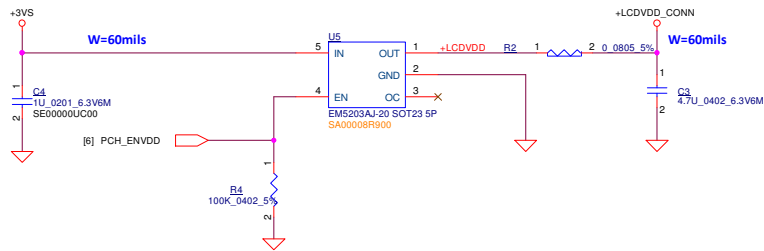
1. Hot available in GB2-64 and GB28-64 packages.
2. GPU debug pins not connected to HBM, see section 7.1.13.

**Notes:**

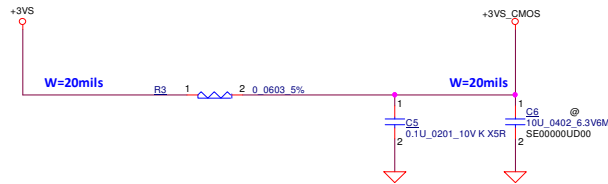
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to URAM. See section 7.1.13.



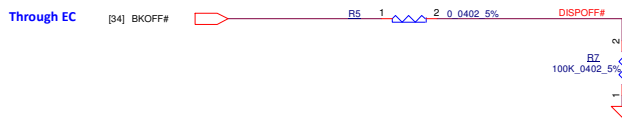
# LCD POWER SWITCH



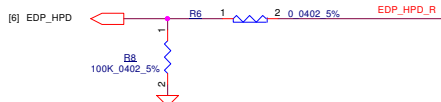
# CAMERA POWER CIRCUIT



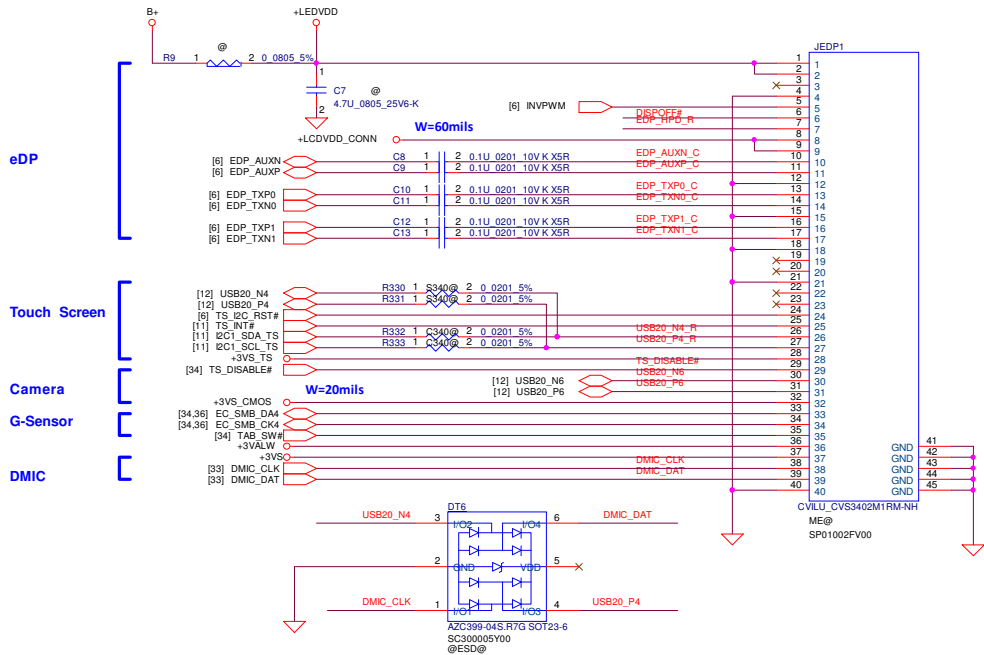
# DISPLAY OFF



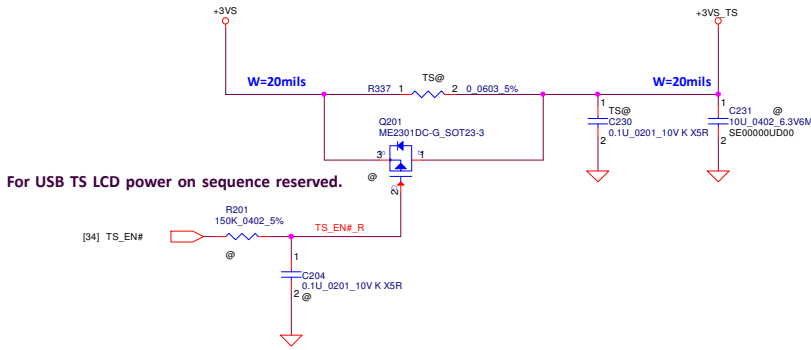
# HOT PLUG DETECT



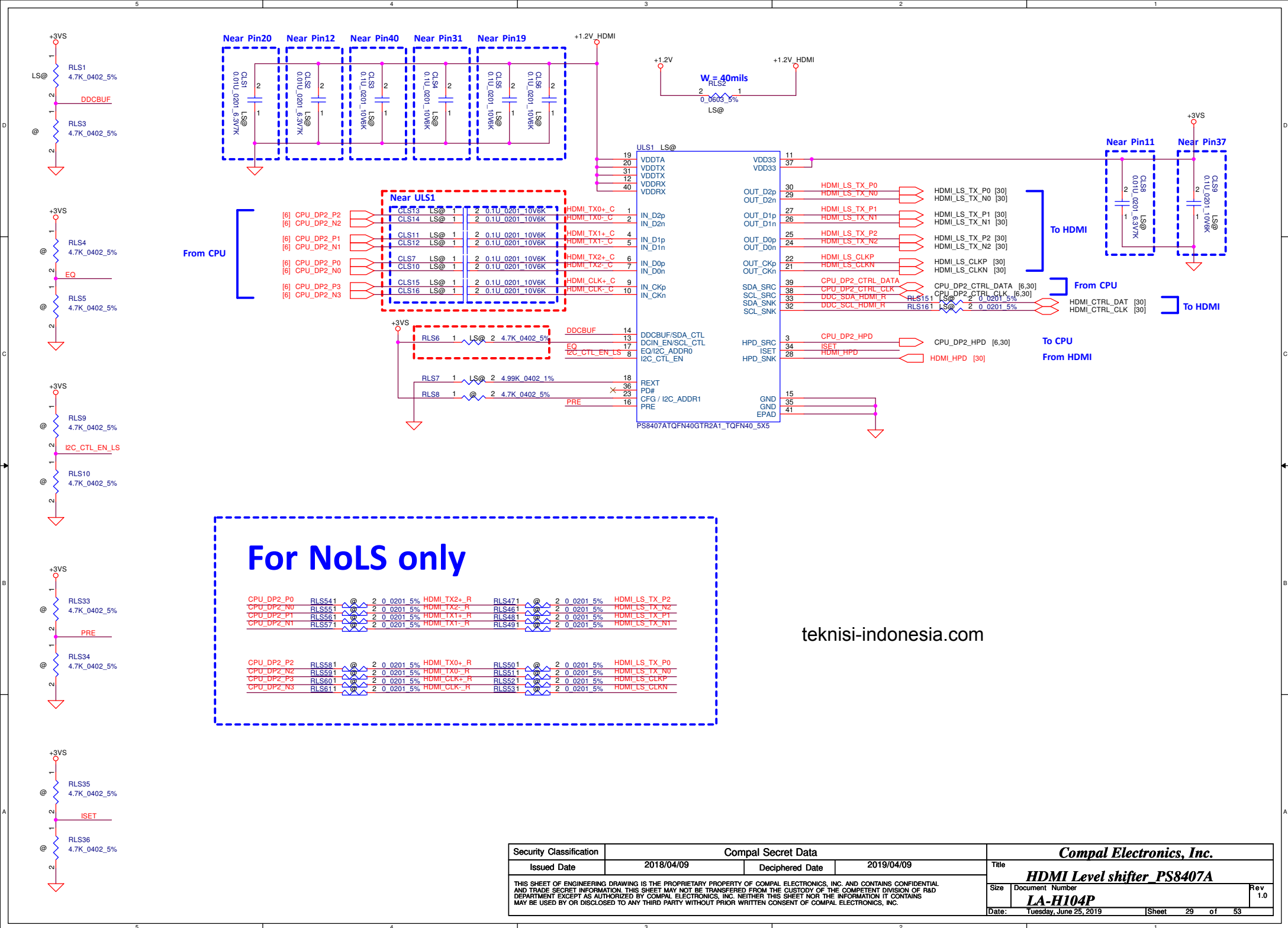
# eDP CONNECTOR



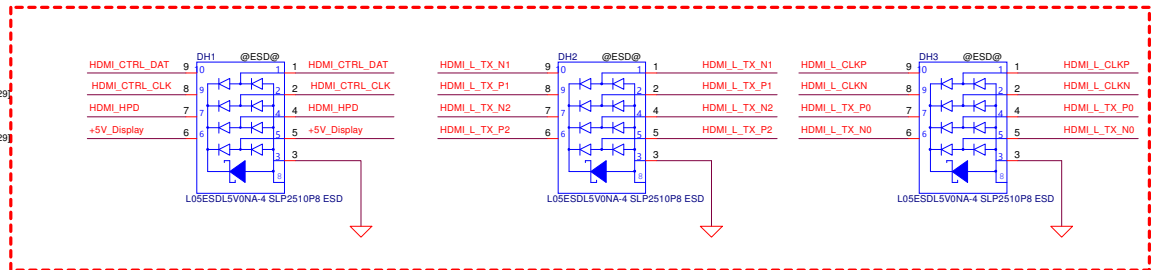
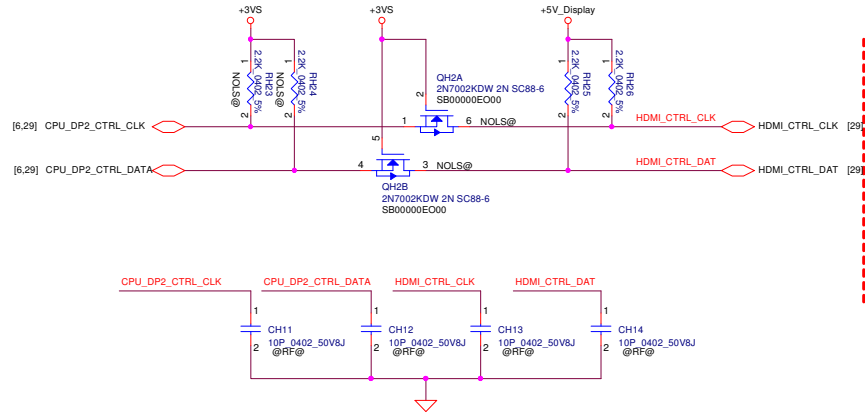
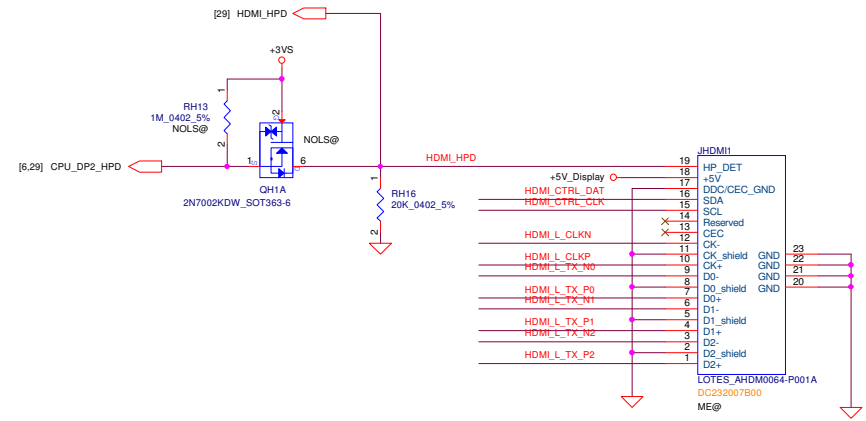
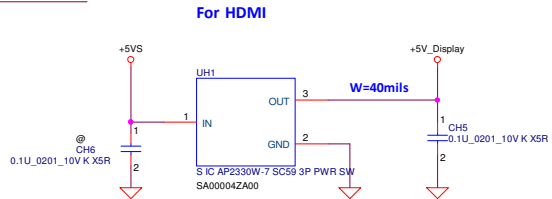
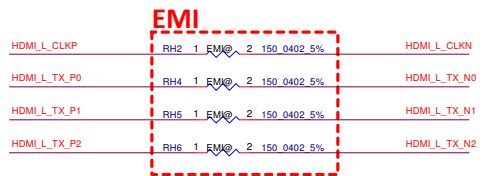
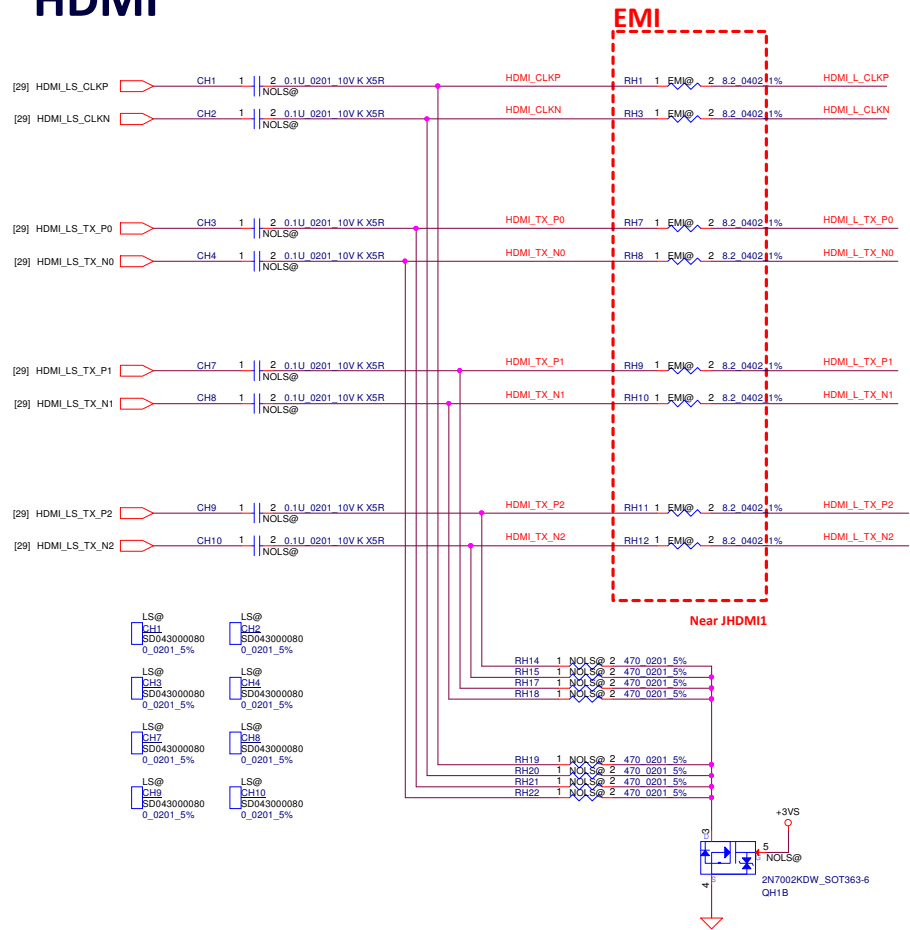
# Touch Screen POWER CIRCUIT



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/04/09		Title	
		Deciphered Date		2019/04/09	
				B P / G m a / M C	
				LA-H104P	
				Rev 1.0	
				Date: Tuesday, June 25, 2019	
				Sheet 28 of 53	



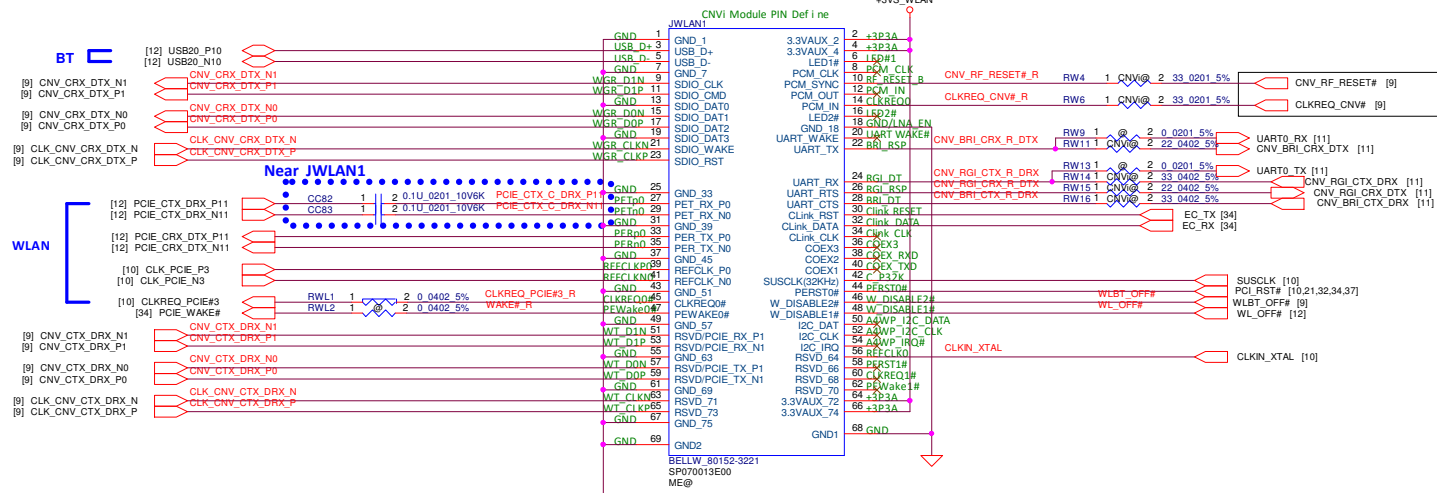
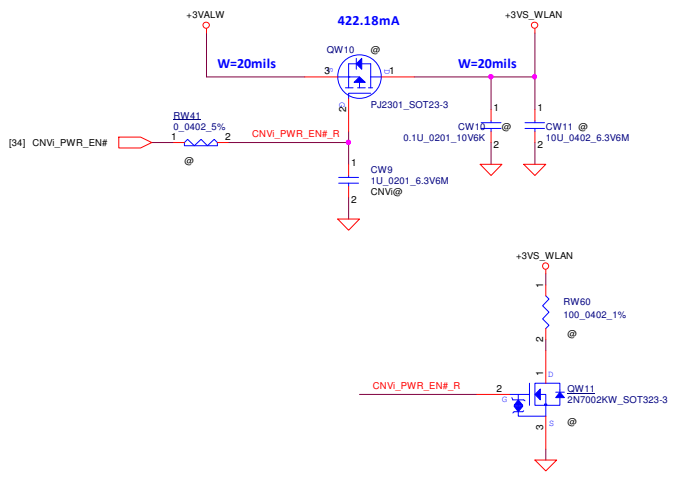
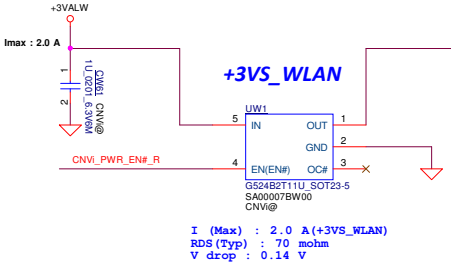
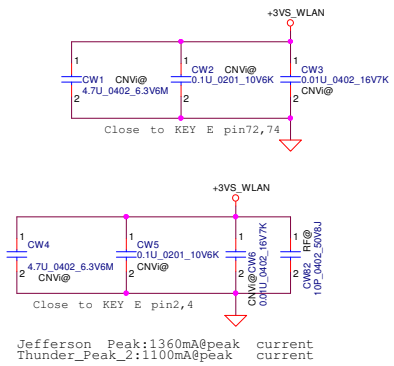
HDMI



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				B M
Size	Document Number	Rev	1.0	
Custom	LA-H104P	Date: Tuesday, June 25, 2019	Sheet	30 of 53

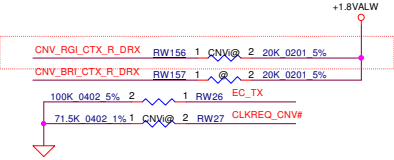
NGFF WLAN /BT(Key E)

NGFF Wireless LAN / BT (Key E) [PCIe+USB/CNVi]



The connectivity module power supply pin shall be connected directly to the rail DSW.  
From  
567240\_Intel\_Wireless\_AC\_9560\_Jefferson\_Peak\_EPS\_Rev1.1

PCH EDS : M.2 CNV Mode Select  
GPP\_F6/CNV\_RGI\_DT  
0 = Integrated CNVi enable.  
1 = Integrated CNVi disable.



Note: The real behavior of BT\_DISABLE are  
BT\_DISABLE=LOW, BT=OFF  
BT\_DISABLE=HIGH, BT=ON

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Rev	1.0
				Date:	Tuesday, June 25, 2019
				Sheet	31 of 53



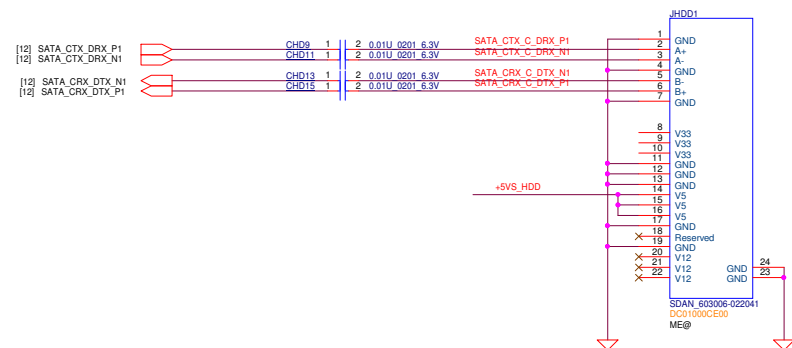
The diagram illustrates the internal wiring of the SSD1 connector. It is organized into three main horizontal sections:

- Top Section (Power and Ground):** Shows connections for +3VSS1, +3VS, and GND. Key components include capacitors C18 (0.01uF, 0.002, 10VTK), C19 (0.1uF, 0.001, 10VTK), C20 (100.00uF, 3.3V6A), and C21 (100.00uF, 3.3V6A). A resistor R10 (0.0605, 5%) is connected between +3VS and GND.
- Middle Section (Data Pins):** Shows connections for PCIe and SATA data lines. Pins are labeled with CC84 through CC91. The connections are as follows:
  - CC84: 2 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_N13
  - CC85: 7 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_P13
  - CC86: 1 1 2 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_N14
  - CC87: 2 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_P14
  - CC88: 1 1 2 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_N15
  - CC89: 2 0.22u 0402 6.3V6K PCIe CTX\_C\_DRX\_P15
  - CC90: 1 1 2 0.22u 0402 6.3V6K SATA CTX\_C\_DRX\_N2
  - CC91: 2 0.22u 0402 6.3V6K SATA CTX\_C\_DRX\_P2
- Bottom Section (Additional Power and Ground):** Shows connections for NGFF\_SSD\_PDET#, SUSCLK(32kHz), and GND1/GND2. The connections are as follows:
  - NGFF\_SSD\_PDET# (Pin 59) to PEDET(NC-PCIe/GND-SATA) (Pin 63)
  - SUSCLK(32kHz) (Pin 60) to 3P3VALX (Pin 62)
  - GND1 (Pin 68) to GND (Pin 69)
  - GND2 (Pin 69) to GND (Pin 68)

The diagram also includes a legend for the components used:

- CC84: 2 0.22u 0402 6.3V6K
- CC85: 7 0.22u 0402 6.3V6K
- CC86: 1 1 2 0.22u 0402 6.3V6K
- CC87: 2 0.22u 0402 6.3V6K
- CC88: 1 1 2 0.22u 0402 6.3V6K
- CC89: 2 0.22u 0402 6.3V6K
- CC90: 1 1 2 0.22u 0402 6.3V6K
- CC91: 2 0.22u 0402 6.3V6K

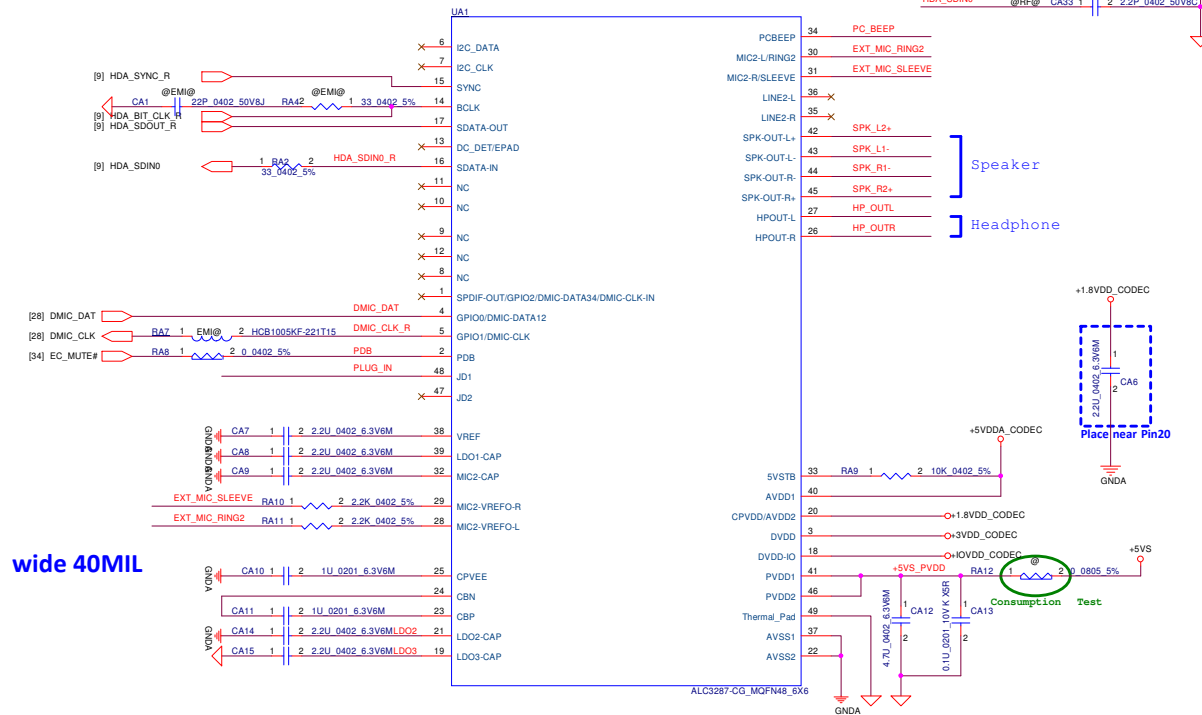
The diagram is a detailed electrical schematic showing the internal connections of the SSD1 connector.



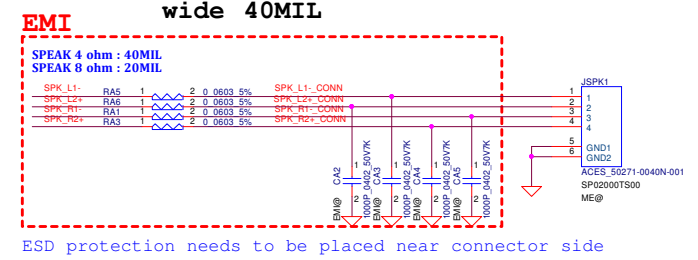
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2018/04/09	Title	SSD/HDD
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev 1.0
				Document Number	
				LA-H104P	
Date:	Tuesday, June 25, 2019	Sheet	32	of	53



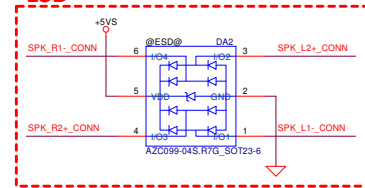
## ALC3287



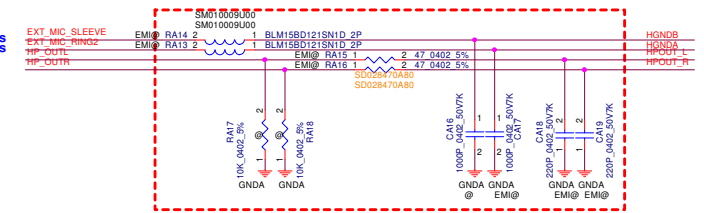
## Speaker



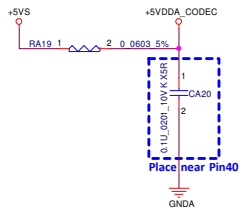
## ESD



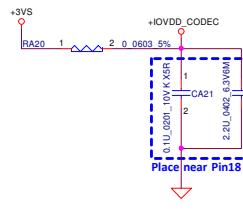
## EMI

W=40mils  
W=40mils

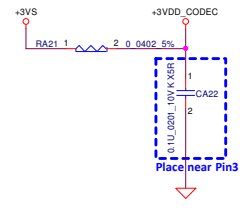
## +5VS --&gt; +5VDDA\_CODEC



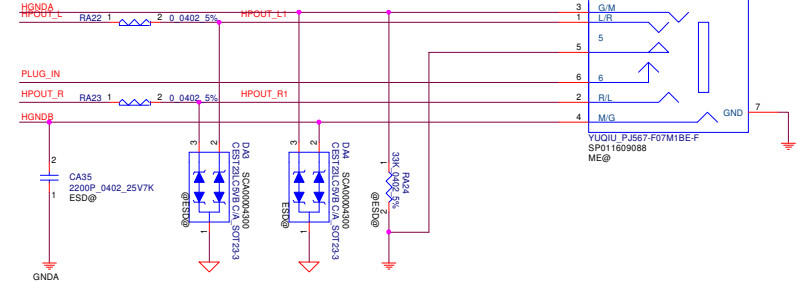
## +3.3VS --&gt; +IOVDD\_CODEC



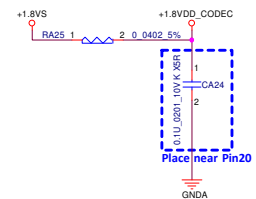
## +3VS --&gt; +3VDD\_CODEC

Combo Jack  
(Normal Open)

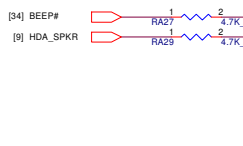
HGND / HGND\_B, W=60mils



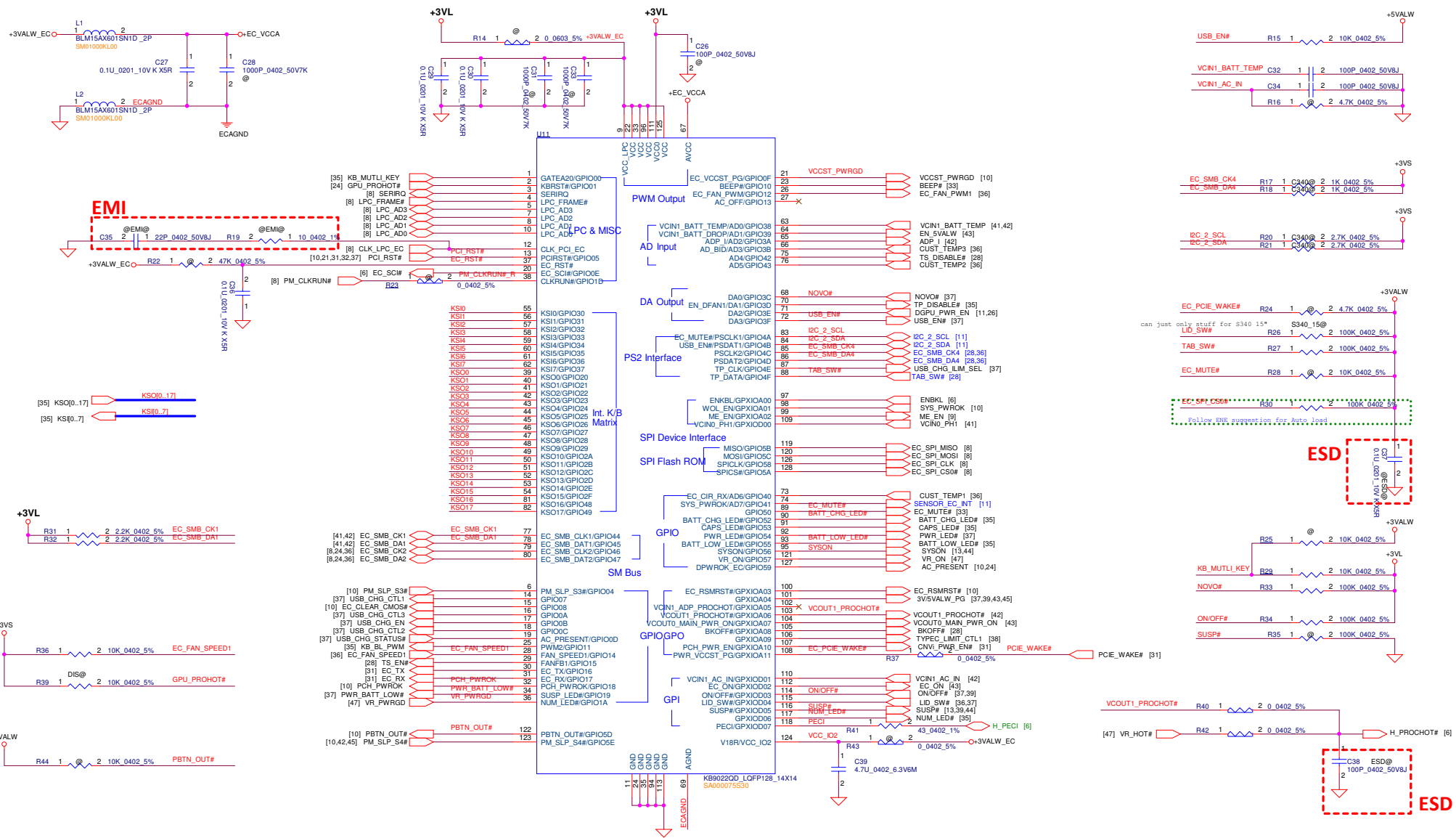
## +1.8VS --&gt; +1.8VDD\_CODEC



## PC BEEP

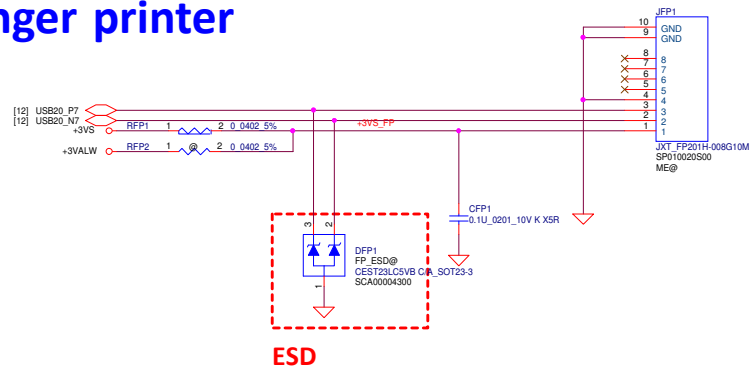


Security Classification	Compal Secret Data	Title	Compal Electronics, Inc.
Issued Date	2018/04/09	Deciphered Date	2019/04/09
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size	Document Number
		Custom	LA-H104P
		Date	Tuesday, June 25, 2019
		Sheet	33 of 33

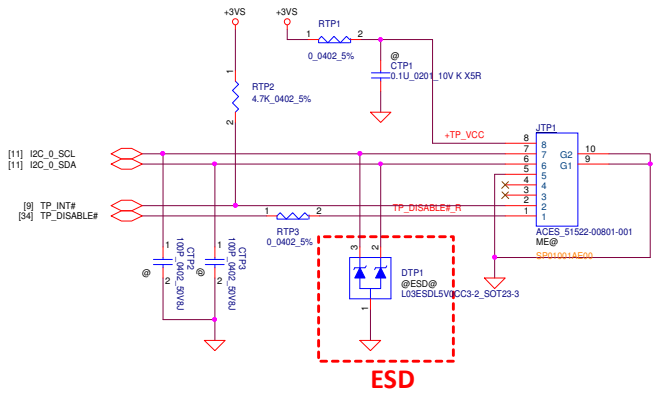


Security Classification		Compal Secret Data		Title	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT, EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	1.0
				LA-H104P	
				Date: Tuesday, June 25, 2019	Sheet 34 of 53

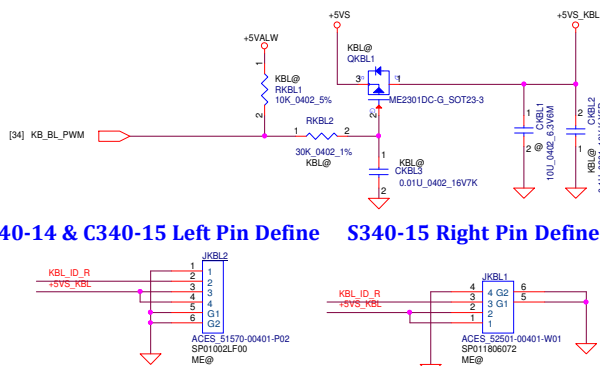
# Finger printer



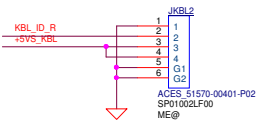
# Touch Pad



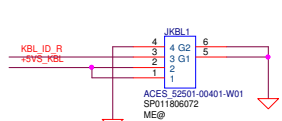
# Keyboard Backlight



## S340-14 & C340-15 Left Pin Define

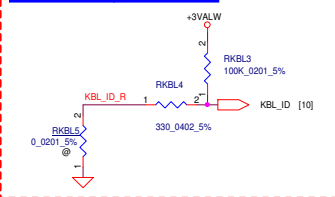


## S340-15 Right Pin Define

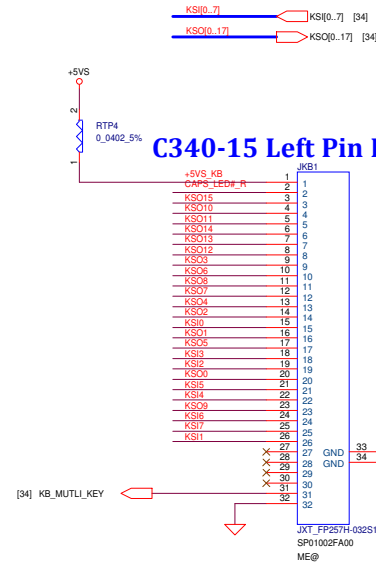


## Keyboard BackLight\_SELECT

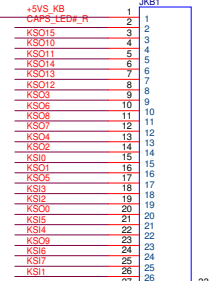
Function	KBL_ID
KBL	0
NO KBL	1



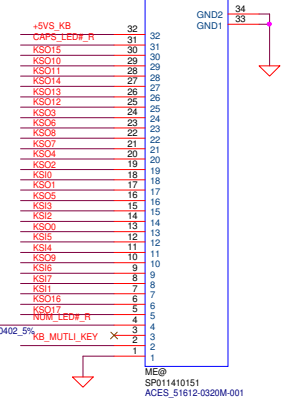
# Keyboard



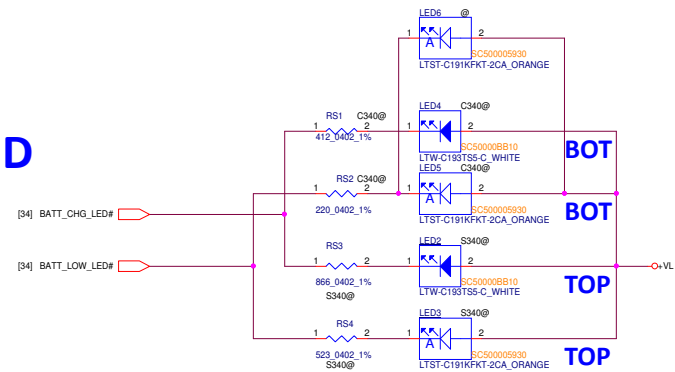
## C340-15 Left Pin Define



## S340-14 & S340-15 Right Pin Define

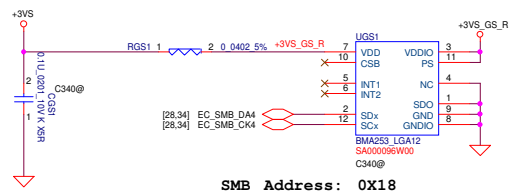


# BATT LED

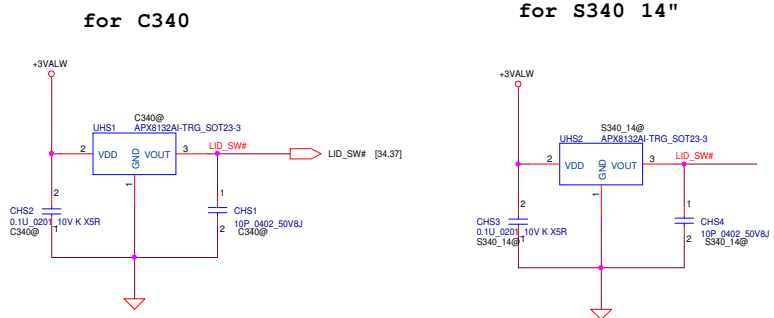


Security Classification	Compal Secret Data		Title	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	KBL/KBD/LED/TP/HS Conn.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0
Date:	Tuesday, June 25, 2019	Sheet	35	of 53

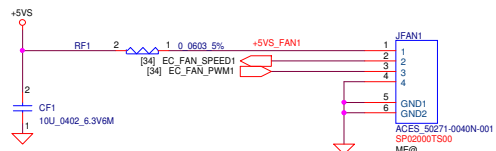
## G-Sensor



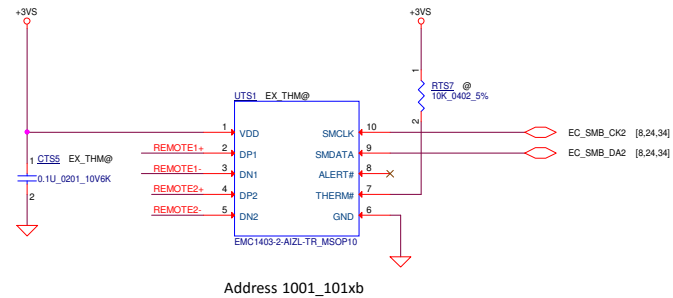
## Hall Sensor



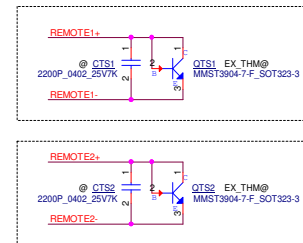
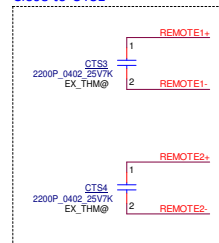
**FAN**



## Thermal Sensor



Close to UTS1

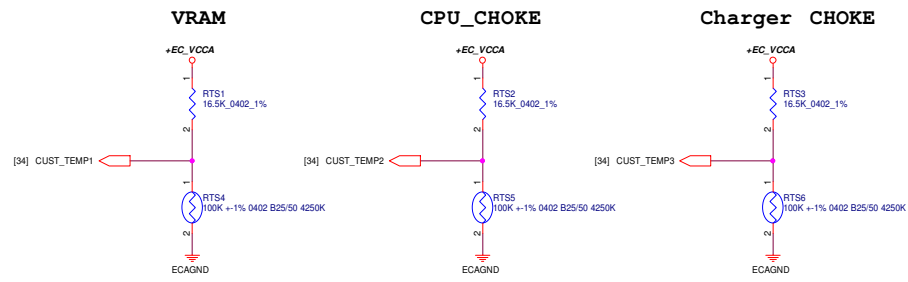


Close to VRAM

Close to Charger CHOKES

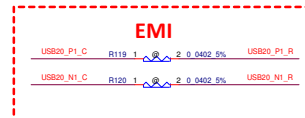
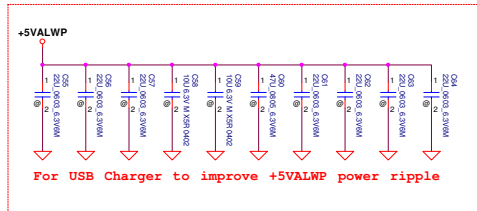
REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

## THERMISTOR

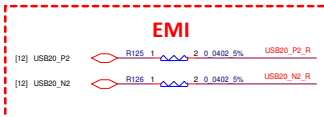
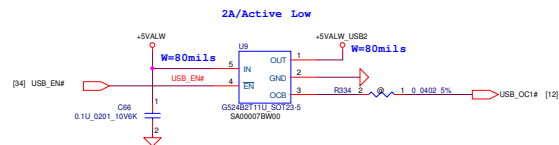


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	<b>FAN / Thermal Sensor</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D MANAGEMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					<b>LA-H104P</b>
				Date: Tuesday, June 25, 2019	Sheet 36 of 53

### USB3.0\_Port (Non-AOU\_Port)

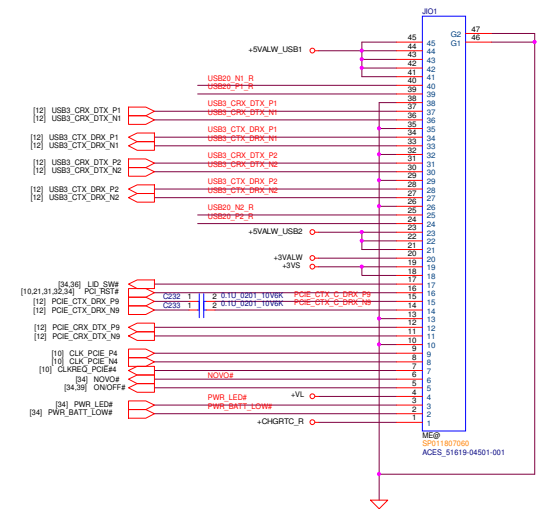



### USB3.0\_Port (Non-AOU\_Port)



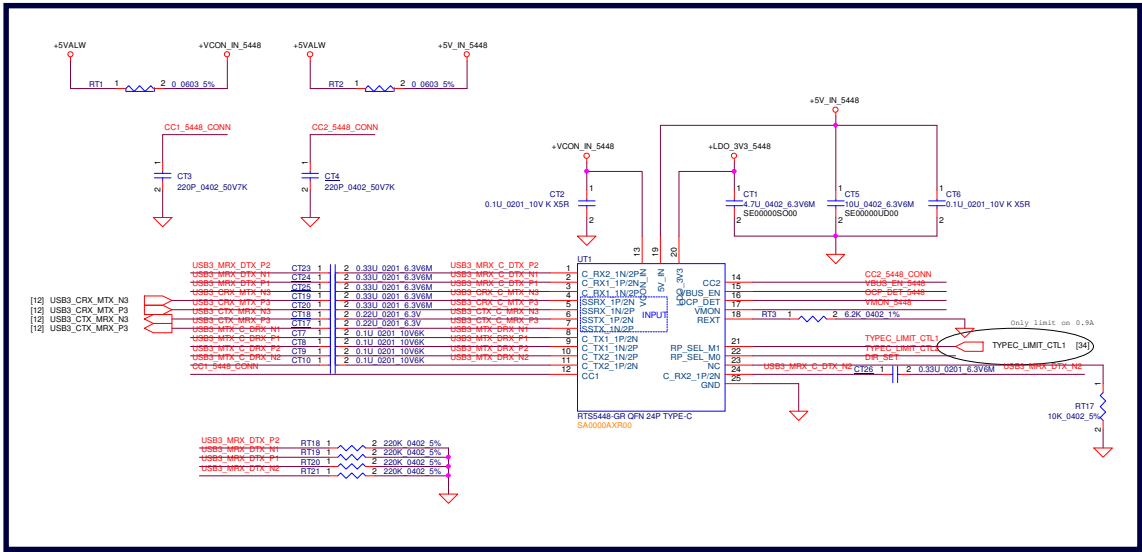
teknisi-indonesia.com

## I/O CONN

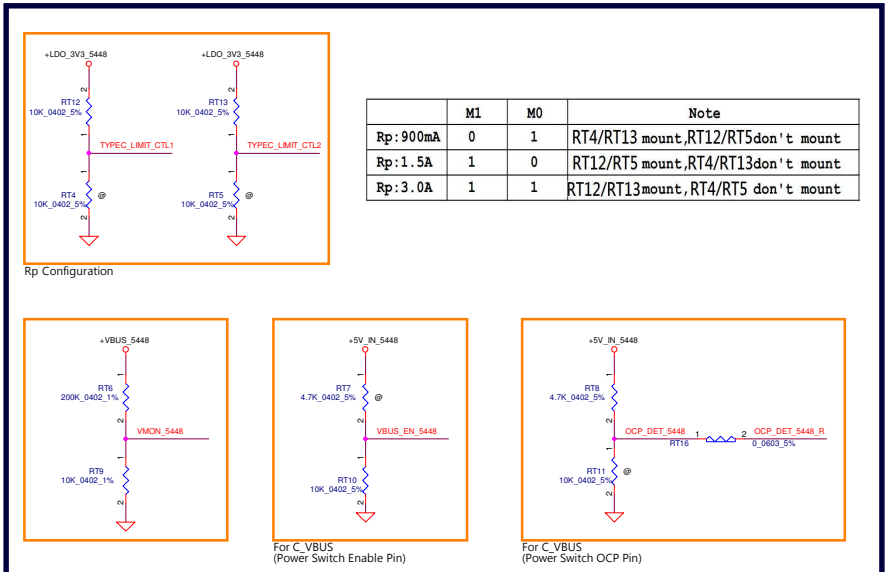


Security Classification	Compul Secret Data		<div>  </div>	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	<div>             Title              IO board           </div>
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPERTY OF COMPUL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND PROPRIETARY INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPUL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPUL ELECTRONICS, INC.			Size	Document Number
			Date	LA-H104P
			Date: <u>Tuesday, June 25, 2019</u>	Sheet <u>37</u> of <u>53</u>

# TYPE-C - CC+MUX (RTS5448-GR)



# MUX MISC.

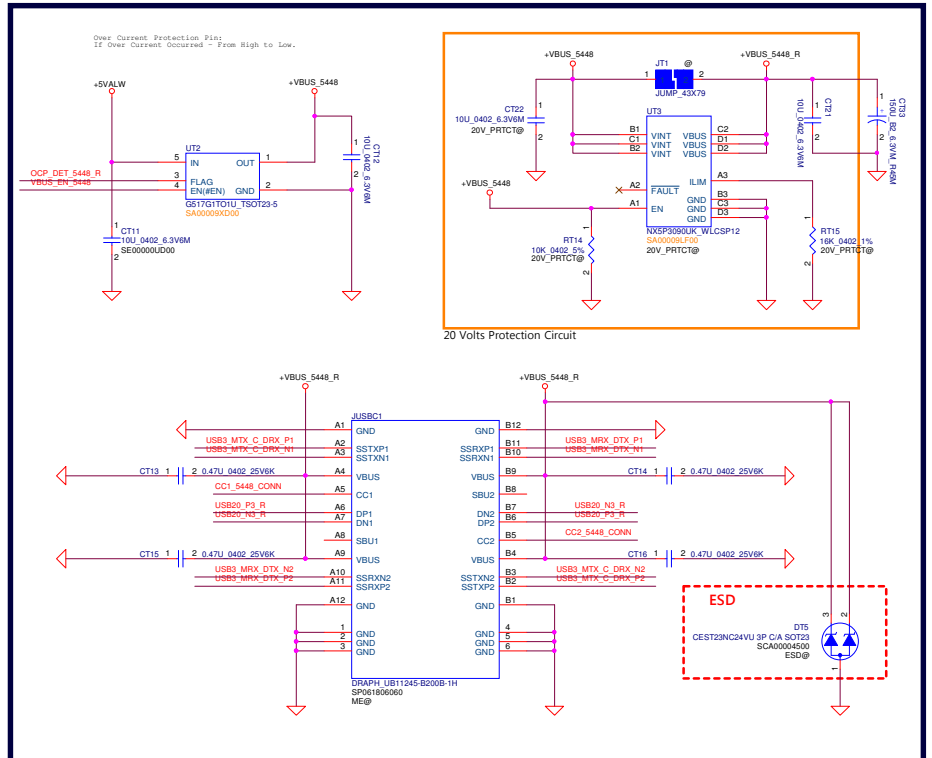


Power switch enable pin	Note
Low Active	RT7/RT10 mount
High Active	RT10 mount, RT7 don't mount

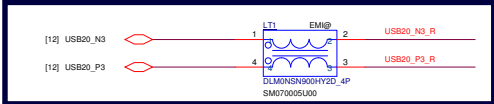
  

Power switch OCP pin	Note
Low Active	RT8/RT11 mount
High Active	RT11 mount, RT8 don't mount

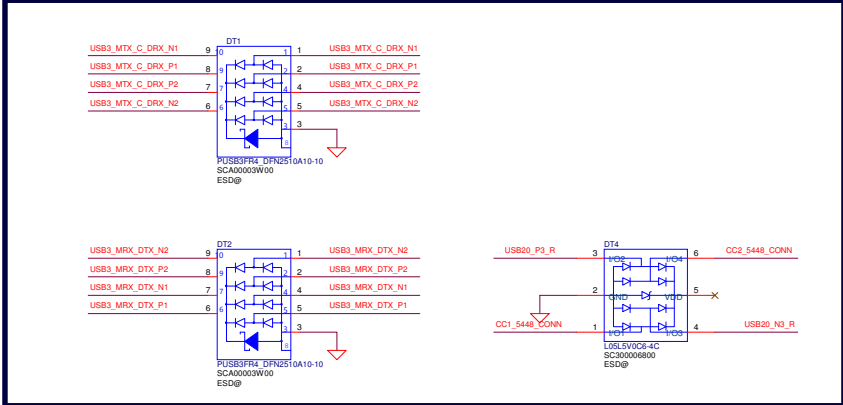
# TYPE-C CONNECTOR



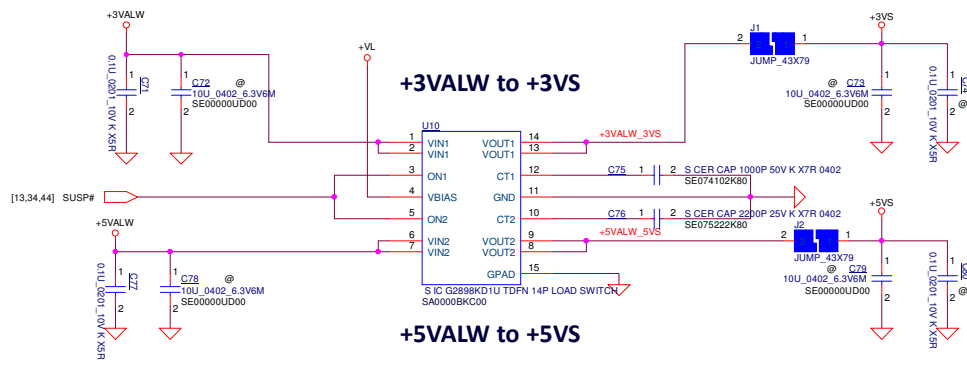
# USB2.0



# ESD COMPONENTS

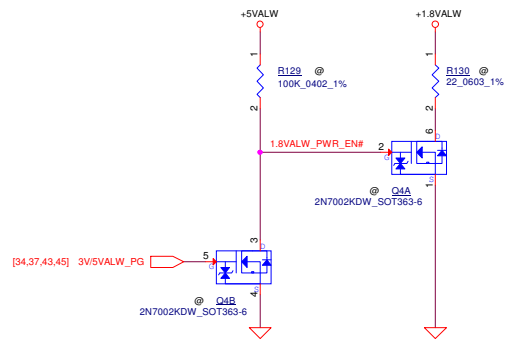


DC to DC

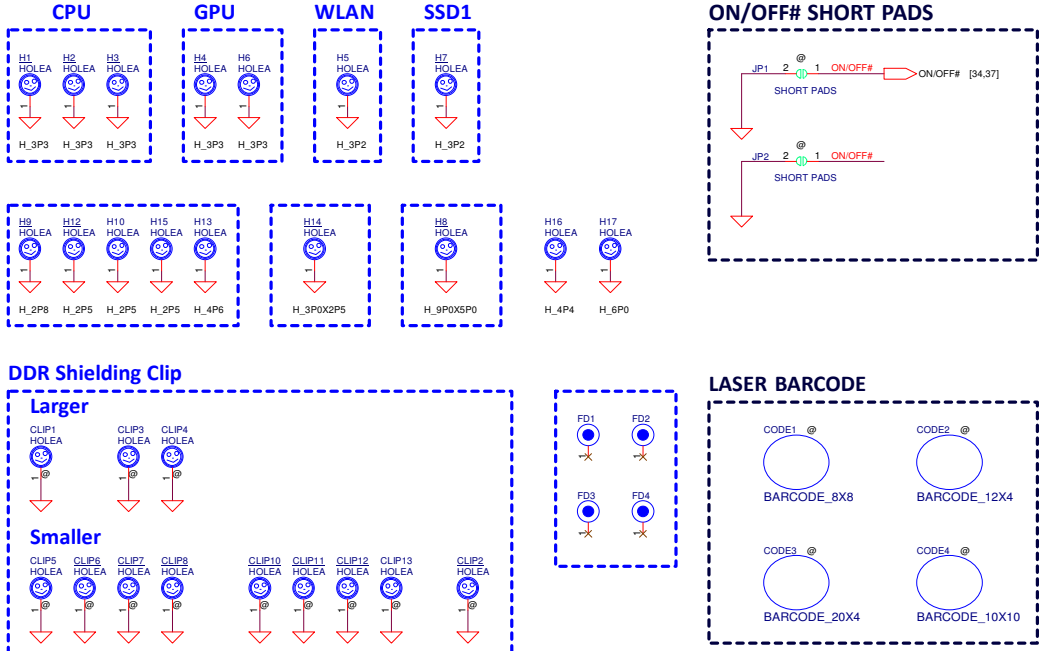


DISCHARGE CIRCUIT

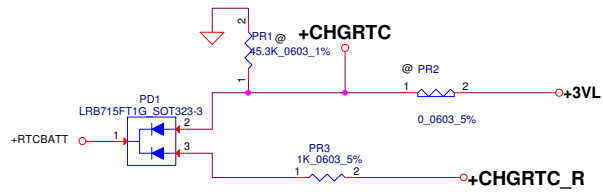
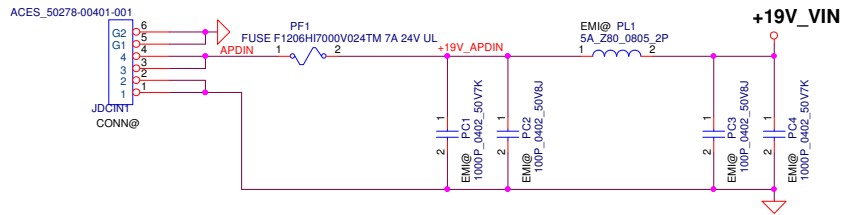
For +1.8VALW Discharge



MISC.

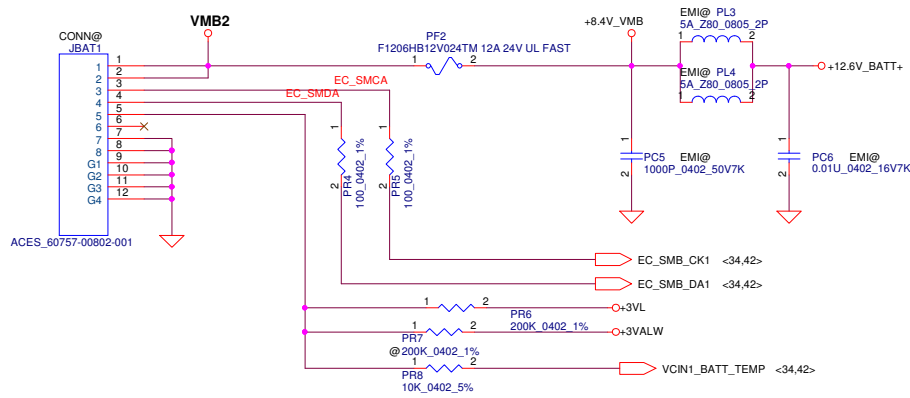


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	DC to DC / Discharge / MISC	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	LA-H104P
				Date:	Tuesday, June 25, 2019
				Sheet	39 of 53
				Rev	1.0

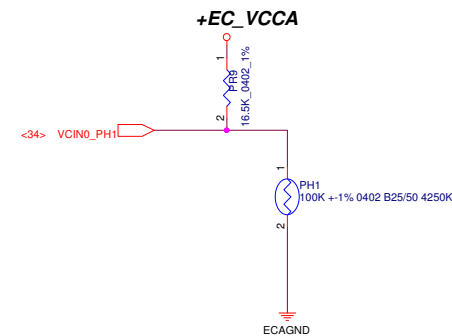


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>PWR- DCIN / Vin Detector</b>	
				Size Custom	Document Number <b>KBL</b>
				Date: Tuesday, June 25, 2019	Rev 1.0
				Sheet 40 of 53	





**PH201 under CPU botten side :**  
**CPU thermal protection at 93 +/-3 degree C**  
**Recovery at 56 +/-3 degree C**



# Protection for reverse input

Vgs = 20V  
Vds = 60V  
Id = 250mA

Rds(on) = 15.8mohm max  
Vgs = 20V  
Vds = 30V  
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W; 0.12W for 65W system; 0.05W for 45W  
CSR rating: 1W  
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

+19V\_VIN

PR729 and PR732 are ACDET set ting base on your project to set

0x3CH <BIT9> PSYS current gain  
Rsl = 10mΩ and Rs2 = 5mΩ or Rsl = 10mΩ and Rs2 = 1mΩ  
BIT0 = 1.14uA/W  
BIT1 = 0.285uA/W  
=====

Rsl = 20mΩ and Rs2 = 10mΩ or Rsl = 20mΩ and Rs2 = 2mΩ  
BIT0 = 2.28uA/W  
BIT1 = 0.57uA/W  
=====

Ipsys = KPSYS x ( VAD P + IAD P + VBAT + IBAT )  
R\_Psys = 1.2V / Ipsys  
KPSYS = 1.14uA/W  
adapter wattage = 45W  
Battery wattage = 40Wh  
Ipsys = 1.14 x (45+40) = 96.9uA  
R\_Psys = 1.2V / 96.9uA = 12.3K-ohm.  
=====

adapter wattage = 65W  
Battery wattage = 40Wh  
Ipsys = 1.14 x (65+40) = 119.7uA  
R\_Psys = 1.2V / 96.9uA = 10K-ohm.  
=====

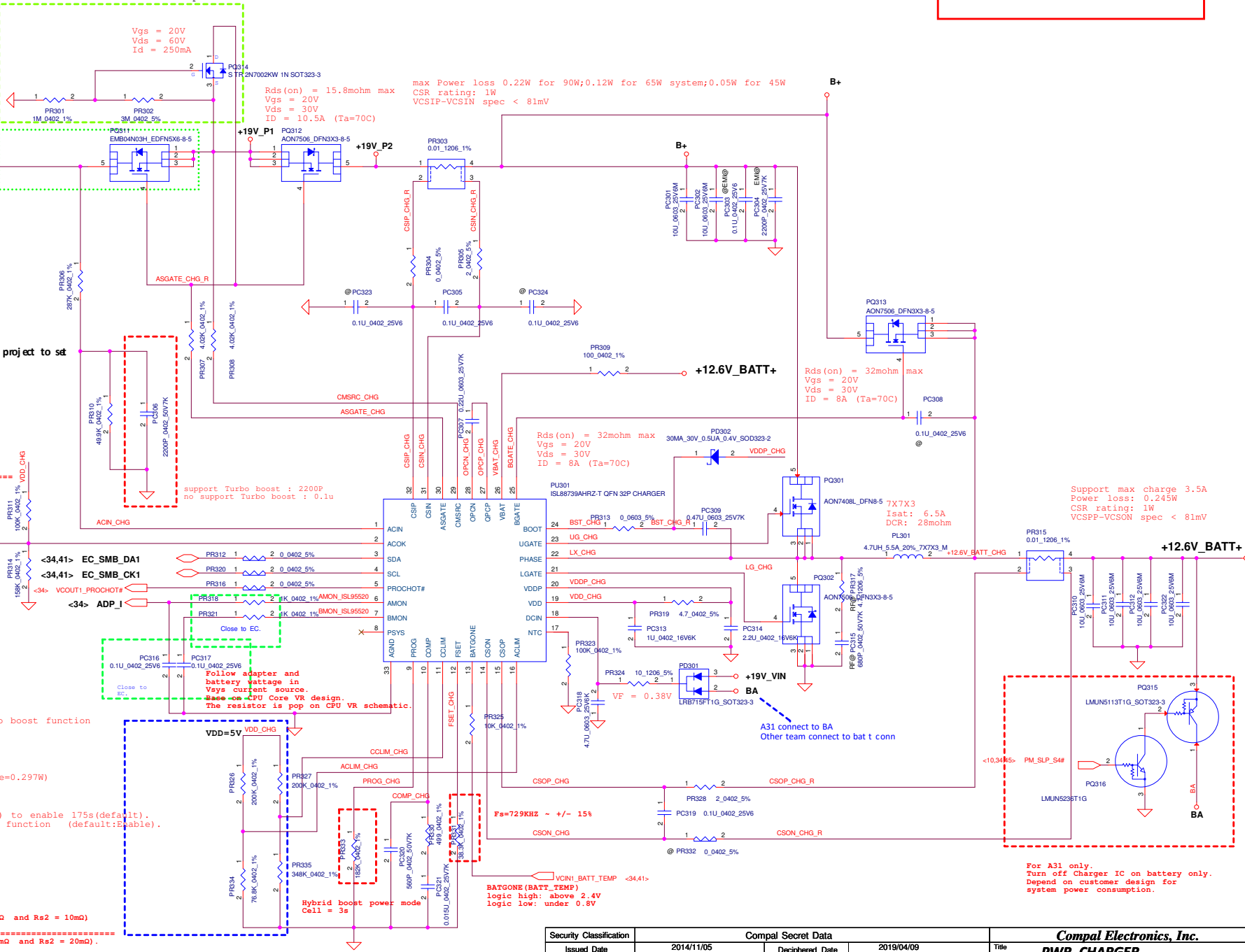
\*\*Design Notes\*\*  
For 45W/65W /90W system, 2S/3S/4S battery  
Maximum Charging current 3.5A  
Maximum Battery discharge power 55W  
#Register Setting  
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function  
2. Disable turbo when AC only  
#Circuit Design  
1. ACLIM and CCLIM are divider voltage control.  
2. Use 7X7 choke and 3X3 H/L side MOSFET  
Charge current 3A  
Power loss : 1.79W (H/S=0.227W, L/S=1.2738W, Choke=0.297W)  
Power density : 0.61 (23X16)  
#Protect function  
1. ACOPP : VCC voltage > 24V  
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).  
3. ACOC : 0X3CH bit4 set1 release adapter limit function (default:Enable).  
4. CHOCOP : based on charge current setting  
5. BATOV : 4.6V/Cell  
6. BATLOW : No.  
7. TSHUT : 150C

(Rsl = 10mΩ and Rs2 = 5mΩ or Rsl = 20mΩ and Rs2 = 10mΩ)  
CC\_LIM = VccLIM / 64 x Rs2  
=====

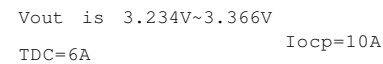
(Rsl = 10mΩ and Rs2 = 10mΩ or Rsl = 20mΩ and Rs2 = 20mΩ).  
CC\_LIM = VccLIM / 32 x Rs2  
=====

AC\_LIM = Vac\_LIM / 32 x Rsl

Battery current limited by CCLim ~ 3.89A.  
Adapter current limited by ACLim ~ 4.33A.  
(PR719 and PQ741 are for change ACLim when AC in)



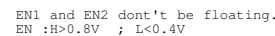
SY8286B\_V3\_single.mdd  
SY8286B\_V3\_dual.mdd



**+3VLP**  **+3VLP**

Vout is 4.998V~5.202V  
TDC=9A                      Iocp>12A

SY8286C\_V3\_single.mdd  
SY8286C\_V3\_dual.mdd



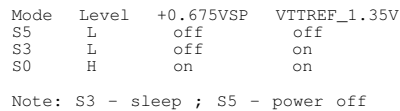
Fsw : 600K Hz

Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>		
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title <b>+3VALW/+5VALW</b>		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev.
				Customer		1.
Date:				Tuesday, June 25, 2019	Sheet 43 of 53	

```
RT8207P_single_V3.mdd    For Single layer
RT8207P_dual_V3.mdd     For Dual layer
```

```
RT8207P_single_V3.mdd    For Single layer
RT8207P_dual_V3.mdd     For Dual layer
```

0.675Volt	+/-	5%
TDC	0.7A	
Peak Current	1A	

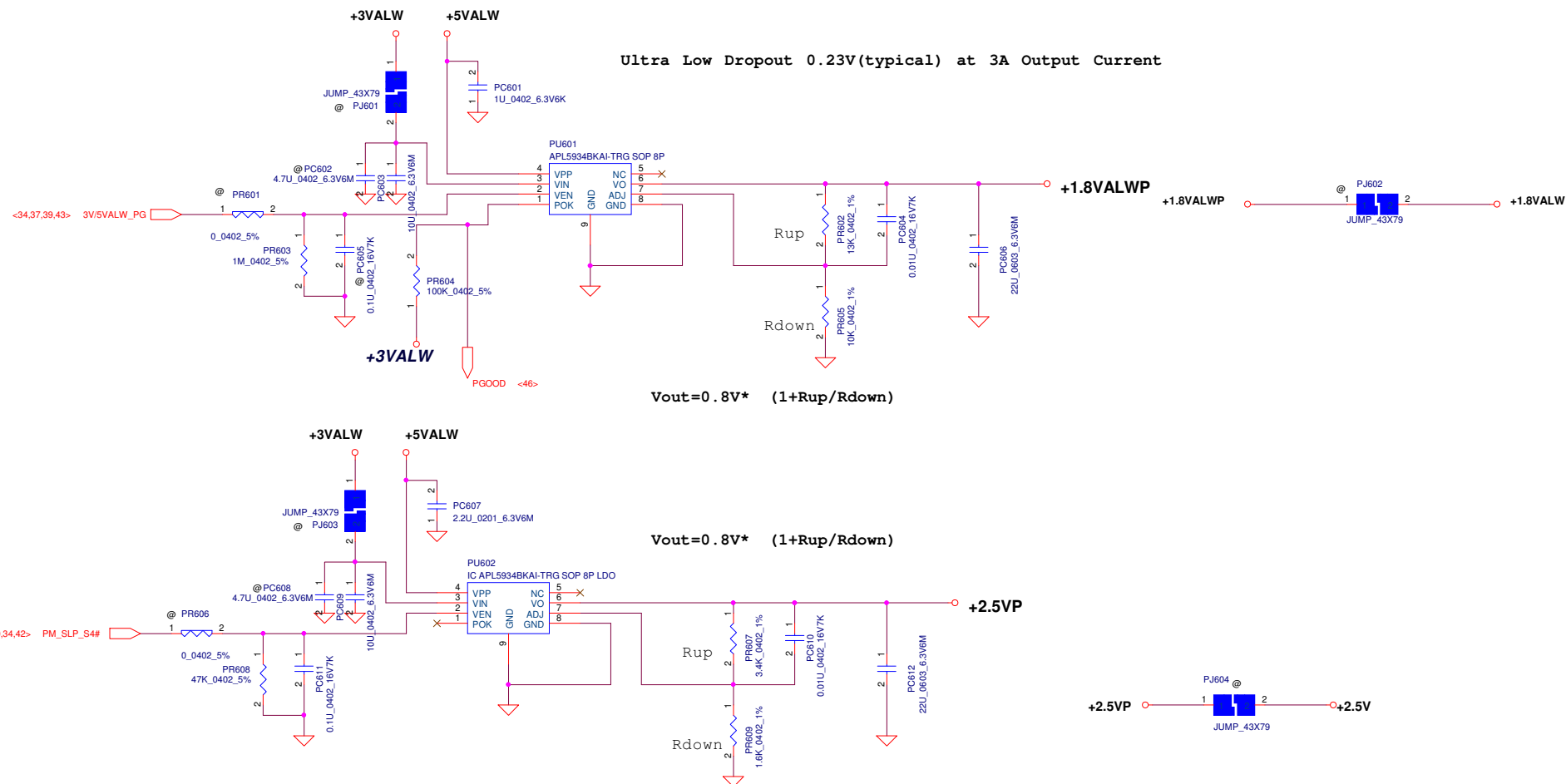


Switching Frequency: 540kHz  
Ipeak=8A  
Iocp~9.6A  
OVP: 113%~120%  
VFB=0.75V, Vout=1.3545V

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	<b>RT8207P</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	
				Date:	Tuesday, June 25, 2019
				Sheet	44 of 53
				Rev	1.0

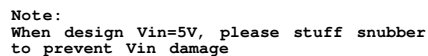
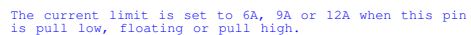
# Module model information

APL5930\_V2.mdd



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	APL5930
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Number
				Custom	KBL
				Date:	Tuesday, June 25, 2019
				Sheet	45 of 53
				Rev	1.0

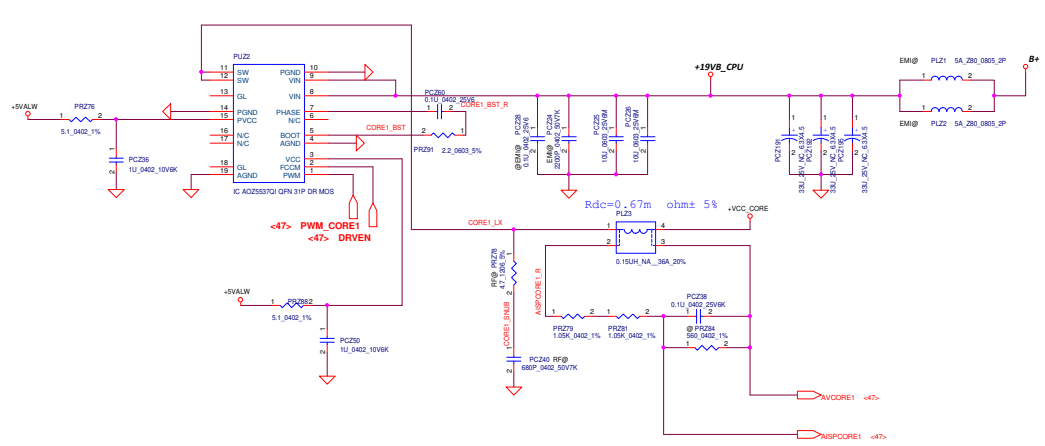
SY8286\_V2\_single.mdd  
SY8286\_V2\_dual.mdd



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>SY8286</b>	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date: Tuesday, June 25, 2019	Sheet 46 of 53







H/S AON6280:  
 R DS (ON) (at V GS =10V) < 6.8m  
 R DS (ON) (at V GS =4.5V) < 10.5m  
 L/S AON6214:  
 R DS (ON) (at V GS =10V) < 2.8m?  
 R DS (ON) (at V GS =4.5V) < 3.5m?

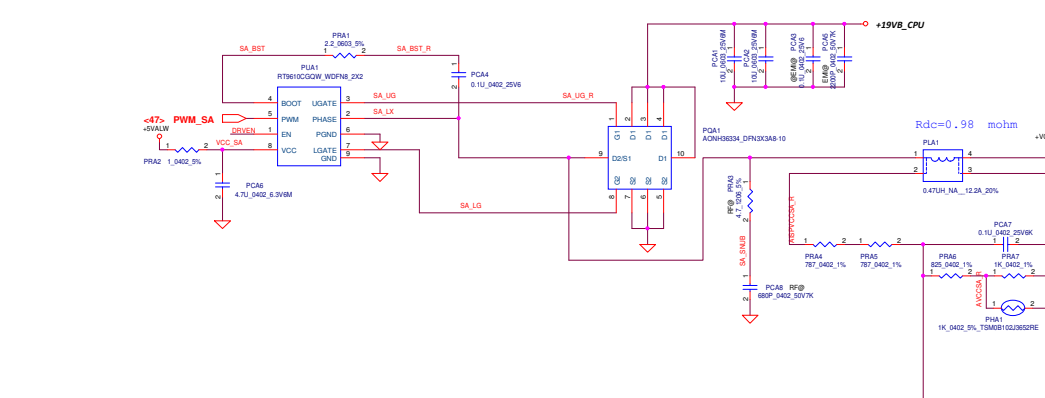
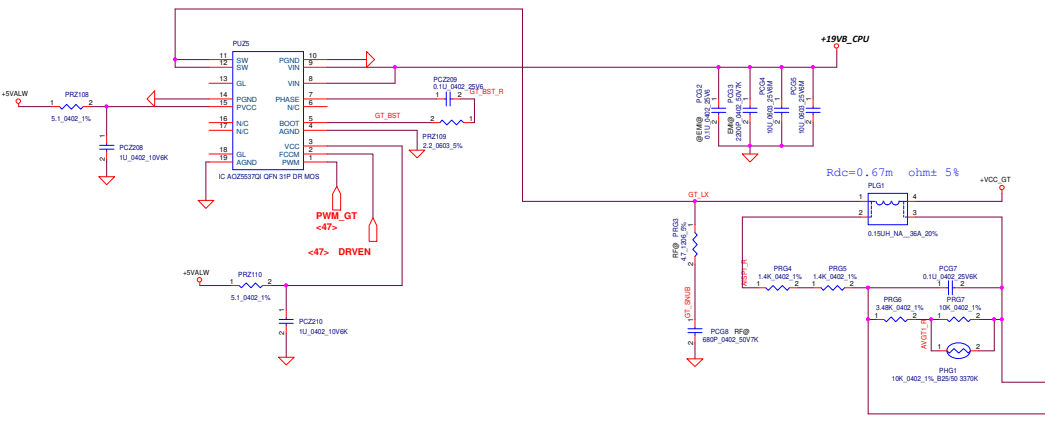
**VCC\_CORE**  
 FSW=450kHz  
 Choke=0.15uH  
 DCR=0.67 mohm +/- 5%

**VCC\_GT**  
 FSW=450kHz  
 Choke=0.15uH  
 DCR=0.67 mohm +/- 5%

**VCC\_SA**  
 FSW=600kHz  
 DCR=6.2 mohm +/- 5%

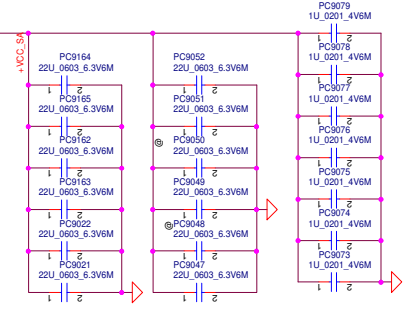
**U22**  
 LI=10.3 mohm  
 TDC=4A  
 ICCMAX=5A  
 OCP=10A

**U42**  
 LI=10.3 mohm  
 TDC=4A  
 ICCMAX=5A  
 OCP=10A



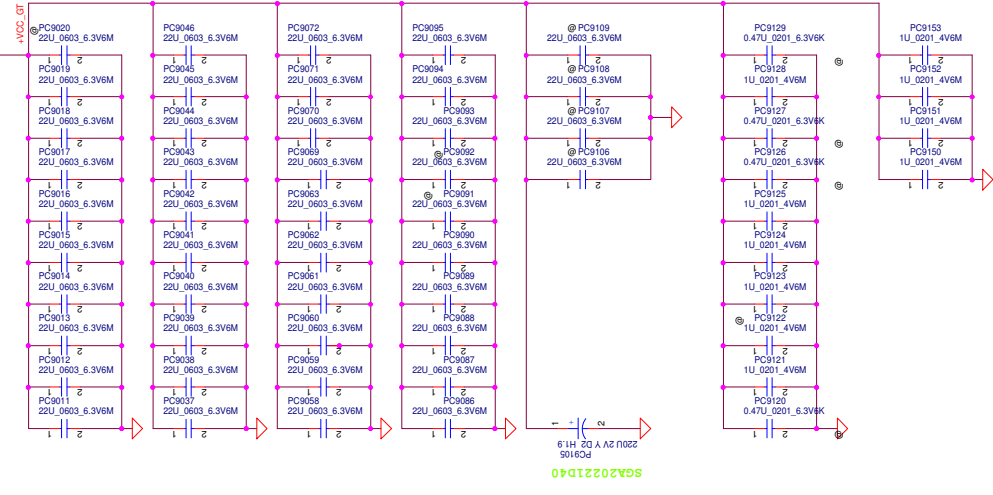
Security Classification		Compel Secret Data		Compel Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	CPU Power stage
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPEL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN CONSENT OF COMPEL ELECTRONICS, INC.				Size	Document Number
				Date	Version
				1/2019	1.0

+VCC\_SA



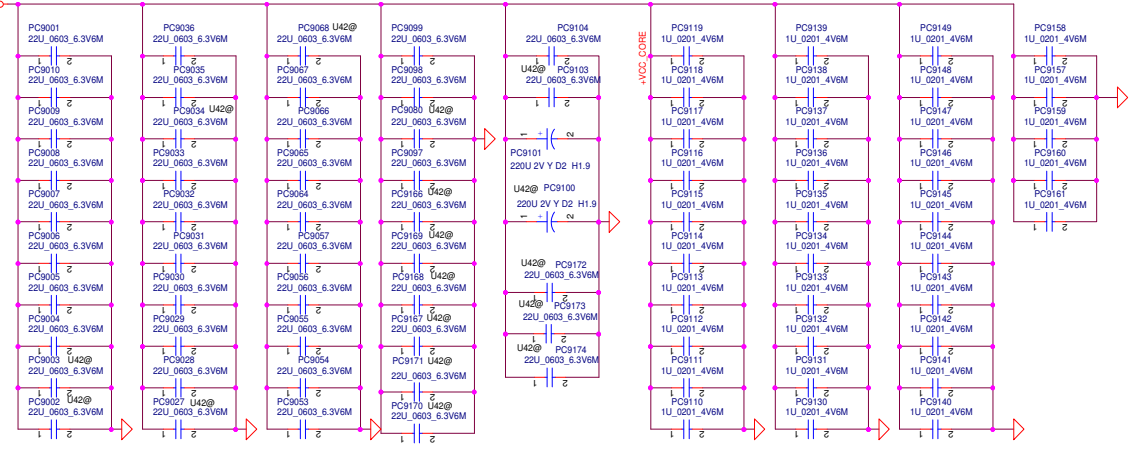
SA  
pop: 22uF\_0603\*10  
1uF\_0201\*7  
unpop: 22uF\_0603\*2

+VCC\_G7



220uF\*1  
22uF\*37  
1uF\*9  
0.47uF\*4  
unpop: 22uF\*7  
1uF\*1

+VCC\_CORE



2018/08/15  
VCORE Output Capacitor:  
U42  
22uF\_0603\*41  
1uF\_0201\*35  
220uF\*2  
UNPOP  
22\_0603\*1

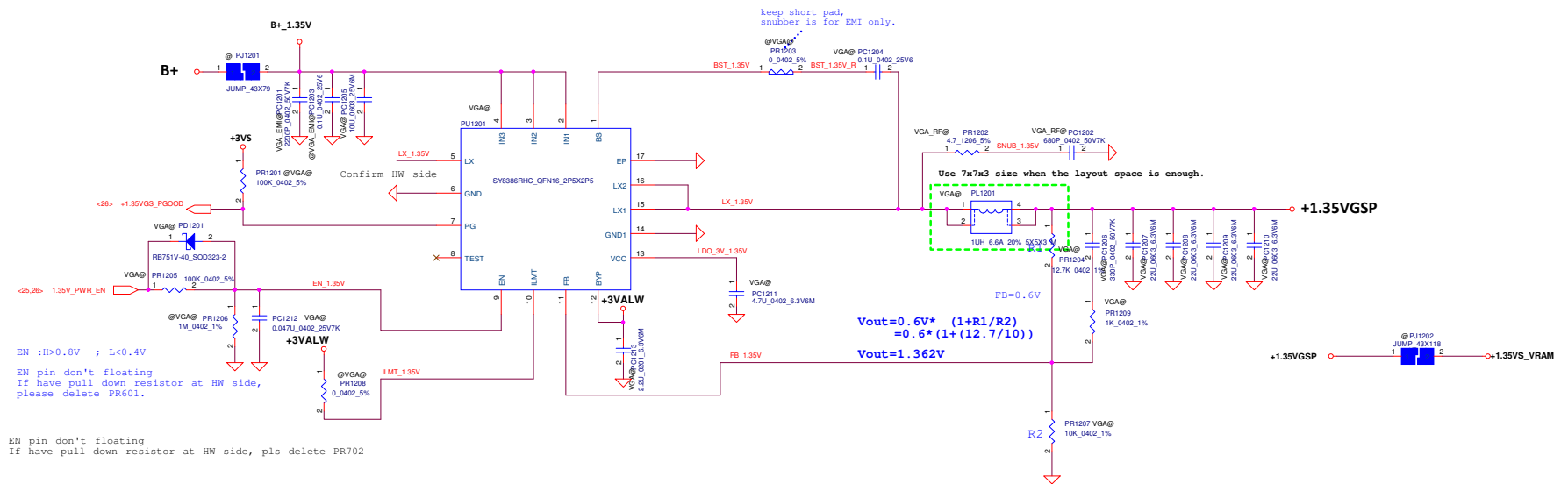
Security Classification			Compal Secret Data		Title	
Issued Date			2018/10/10		2019/04/09	
Dispersed Date					Power Train	
This sheet of drawings remains the property of Compal Electronics, Inc. and contains confidential and trade secret information. This sheet may not be transferred from the competent division of R&D without the written consent of Compal Electronics, Inc. It is to be used only for the purpose intended and may be used by other parties without the written consent of Compal Electronics, Inc.			Size		Document Number	
			C		LA-H104P	
			Rev		1.0	
			Date		1998/08/28/2013	
					48	
					53	

Compal Electronics, Inc.



Module model information

SY8286\_V1\_single.mdd  
SY8286\_V1\_dual.mdd



Security Classification	Compal Secret Data			Title			Compal Electronics, Inc.		
Issued Date	2016/6/2	Deciphered Date	2019/04/09	Size	Document Number	Rev			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THE INFORMATION ON THIS SHEET IS TO BE TRANSMITTED TO ANY OTHER PARTY ONLY BY THE AUTHORIZED PERSONNEL OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	LA-H104P	1.0			
Date:	Tuesday, June 25, 2019			Sheet	51	of	53		

## Version change list (P.I.R. List)

Page 1 of 1 for  
PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For CML CNVI function enhance 0.6A		change PU701 to SY8388RHC	0329	SDV
2	For CML GT power spec request		change PUZ5 PUZ2 PUZ4 to Dr.MOS AOZ5537QI	0329	SDV
3	For charger VDD pin capacitance request		change PC313 PC314 to 2.2uF	0416	SIV
4	For charger DC IN pin capacitance request		change PC318 to 4.7uF	0416	SIV
5				0821	SIV
6				0823	SIV
7				0824	SIV
8				1022	SIT
9				1022	SIT
10				1029	SIT
11				1204	SVT
12				1204	SVT
13				1204	SVT
14				1204	SVT
15				1210	SVT
16					
17					
18					

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (PWR)	
				Size Document Number	
				Custom Z BDW	
Date: Tuesday, June 25, 2019				Sheet	52 of 53
				Rev	1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2018/04/09	Deciphered Date	2019/04/09	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PIR (EE)			
				Size	Document Number	Rev	
				Custym	Z BDW	1.0	
Date:				Tuesday, June 25, 2019	Sheet	53	of 53